


# CB-3 LOGIC SCHEMATICS

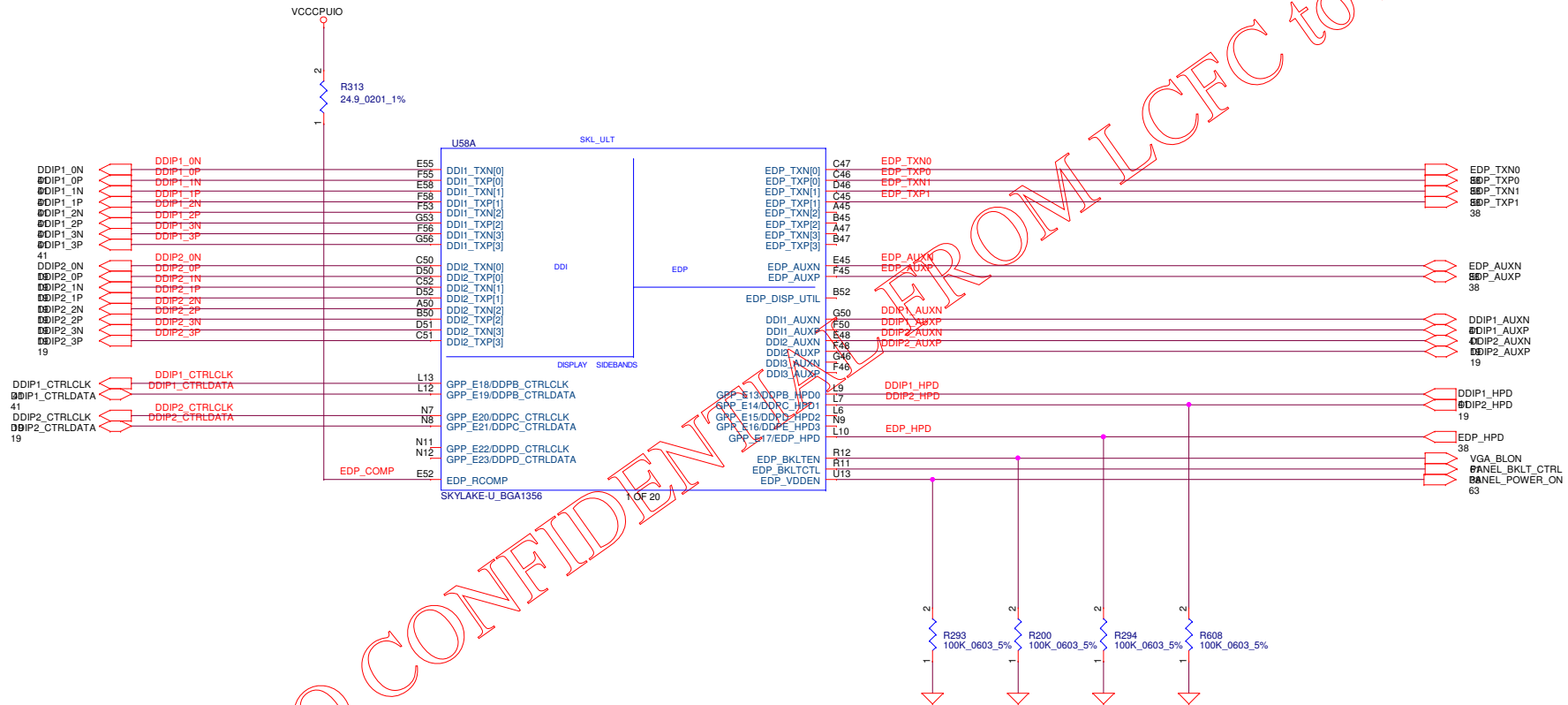
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033.N15S-GM(6/6) : GND	68.G-SENSOR	98.LOAD SW WWAN & WLAN
034.VRAM CHANNEL-A	69.TPM	99.PTH FOR SCREW HOLES
035.BLANK	70.EEPROM/SMBUS SW	100.3rd USB


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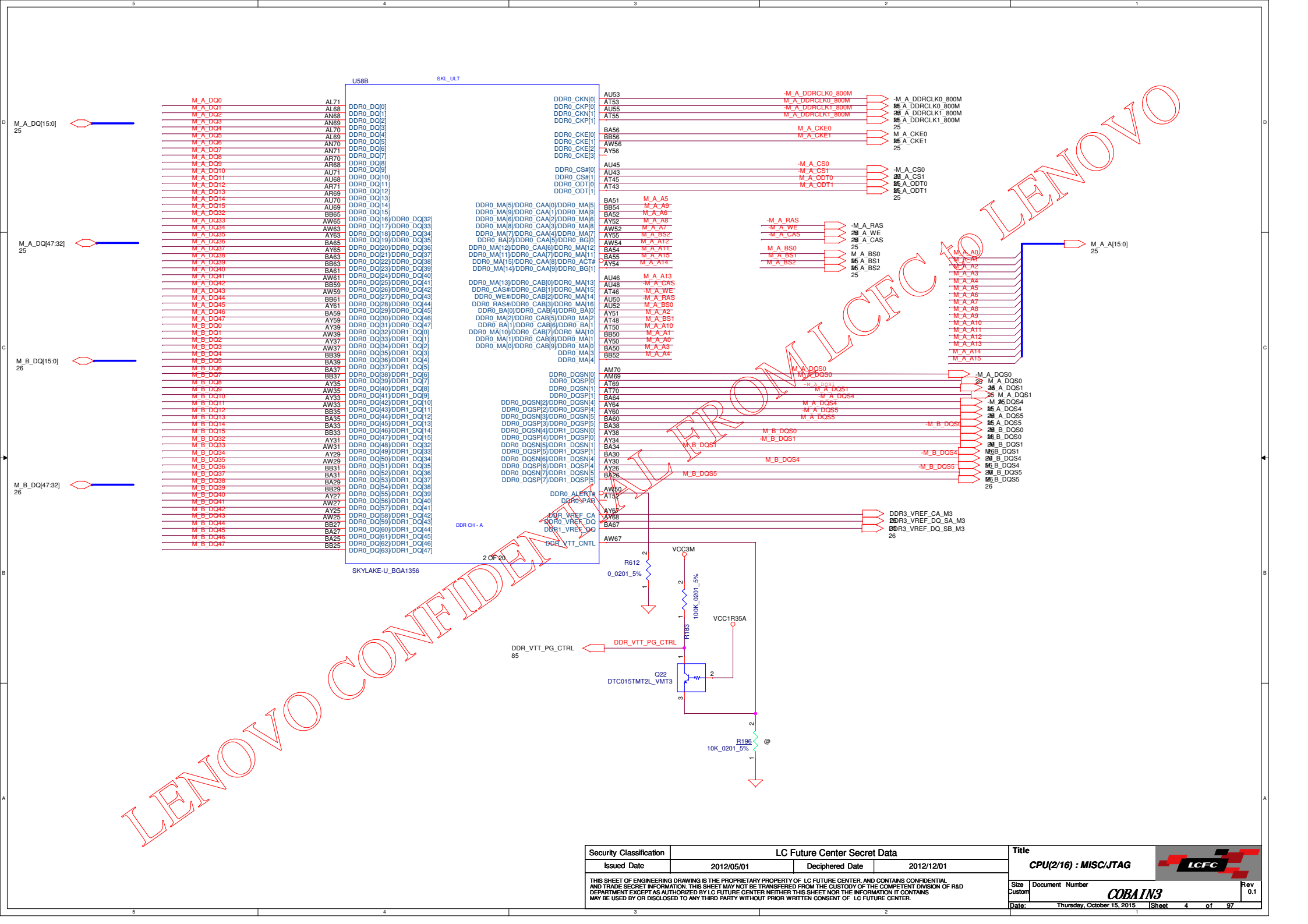
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2012/10/09	CB_1_SWG_SDV_EC011	JV_CB-1_SWG_SDV1_SCH_EC009-010_100801.pdf
2012/10/12	CB_1_SWG_SDV_EC012	JV_CB-1_SWG_SDV1_SCH_EC010-011_101101.pdf
2012/10/13	CB_1_SWG_SDV_EC013	JV_CB-1_SWG_SDV1_SCH_EC011-012_101201.pdf
2012/10/16	CB_1_SWG_SDV_EC014	JV_CB-1_SWG_SDV1_SCH_EC013_101501.pdf
2012/10/17	CB_1_SWG_SDV_EC015	JV_CB-1_SWG_SDV1_SCH_EC014_101601.pdf
2012/10/18	CB_1_SWG_SDV_EC016	JV_CB-1_SWG_SDV1_SCH_EC015_101701.pdf
2012/10/19	CB_1_SWG_SDV_EC017	JV_CB-1_SWG_SDV1_SCH_EC016_101801.pdf
2012/10/20	CB_1_SWG_SDV_EC018	JV_CB-1_SWG_SDV1_SCH_EC017_101901.pdf
2012/10/25	CB_1_SWG_SDV_EC018-022	JV_CB-1_SWG_SDV1_SCH_EC018-021_102401.pdf
2012/10/31	CB_1_SWG_SDV_EC023	JV_CB-1_SWG_SDV1_SCH_EC022_103001.pdf
2012/10/32	CB_1_SWG_SDV_EC023-025	JV_CB-1_SWG_SDV1_SCH_EC023-024_103101.pdf
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2012/11/23	CB_1_SWG_SDV_EC033-036	JV_CB-1_SWG_SDV1_SCH_EC025-035_112201.pdf
2012/11/27	CB_1_SWG_SDV_EC037	JV_CB-1_SWG_SDV1_SCH_EC036_112601.pdf
2012/12/05	CB_1_SWG_SDV_EC037-039	JV_CB-1_SWG_SDV1_SCH_EC037-038_120401.pdf

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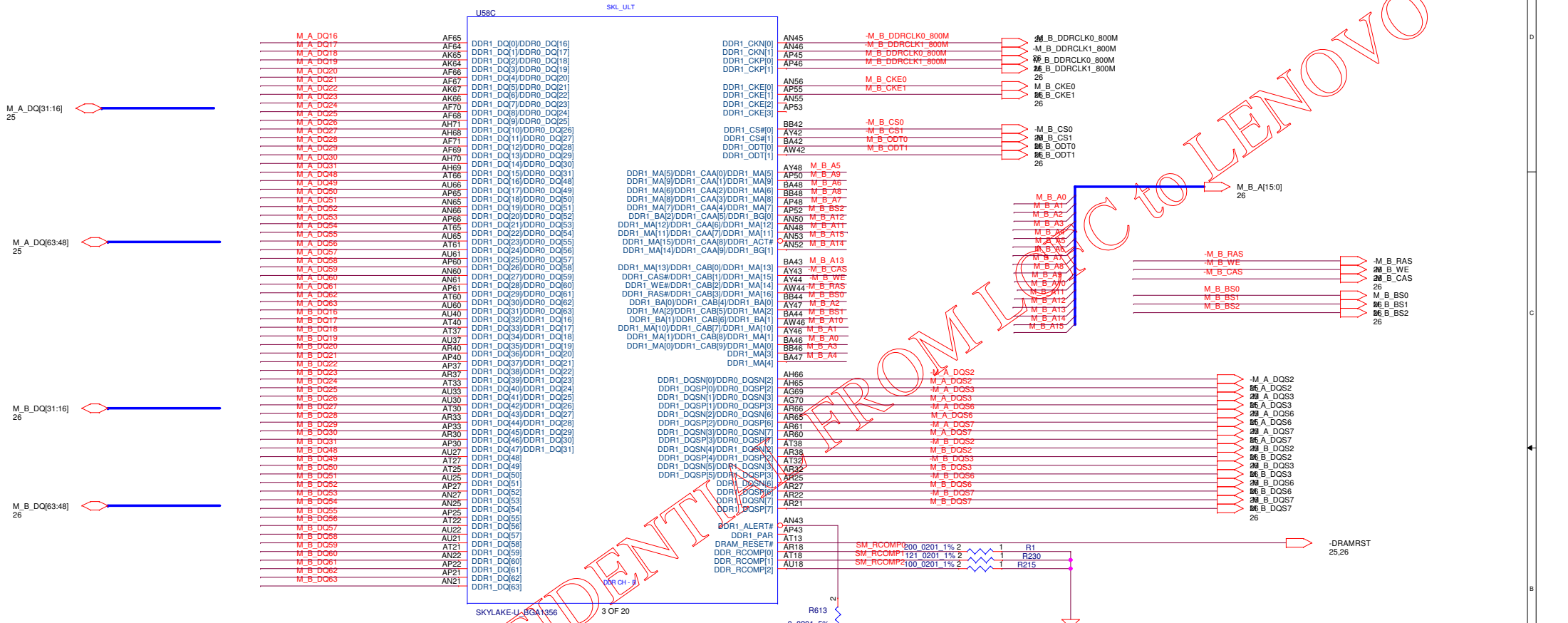


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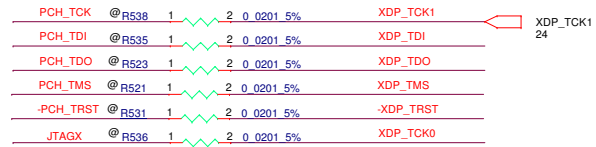
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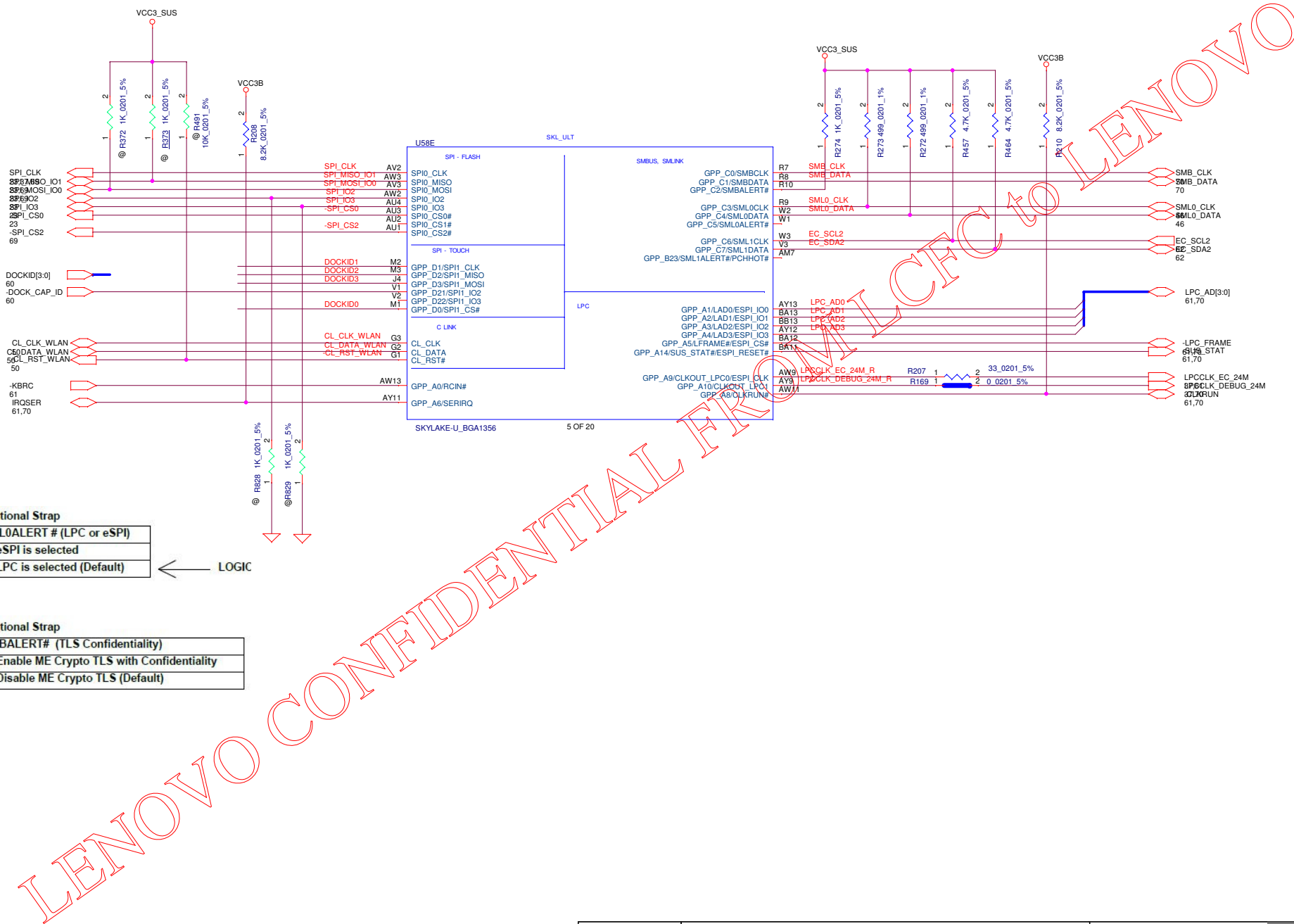


TABLE : Functional Strap

GPP_C5/SML0ALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)



GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

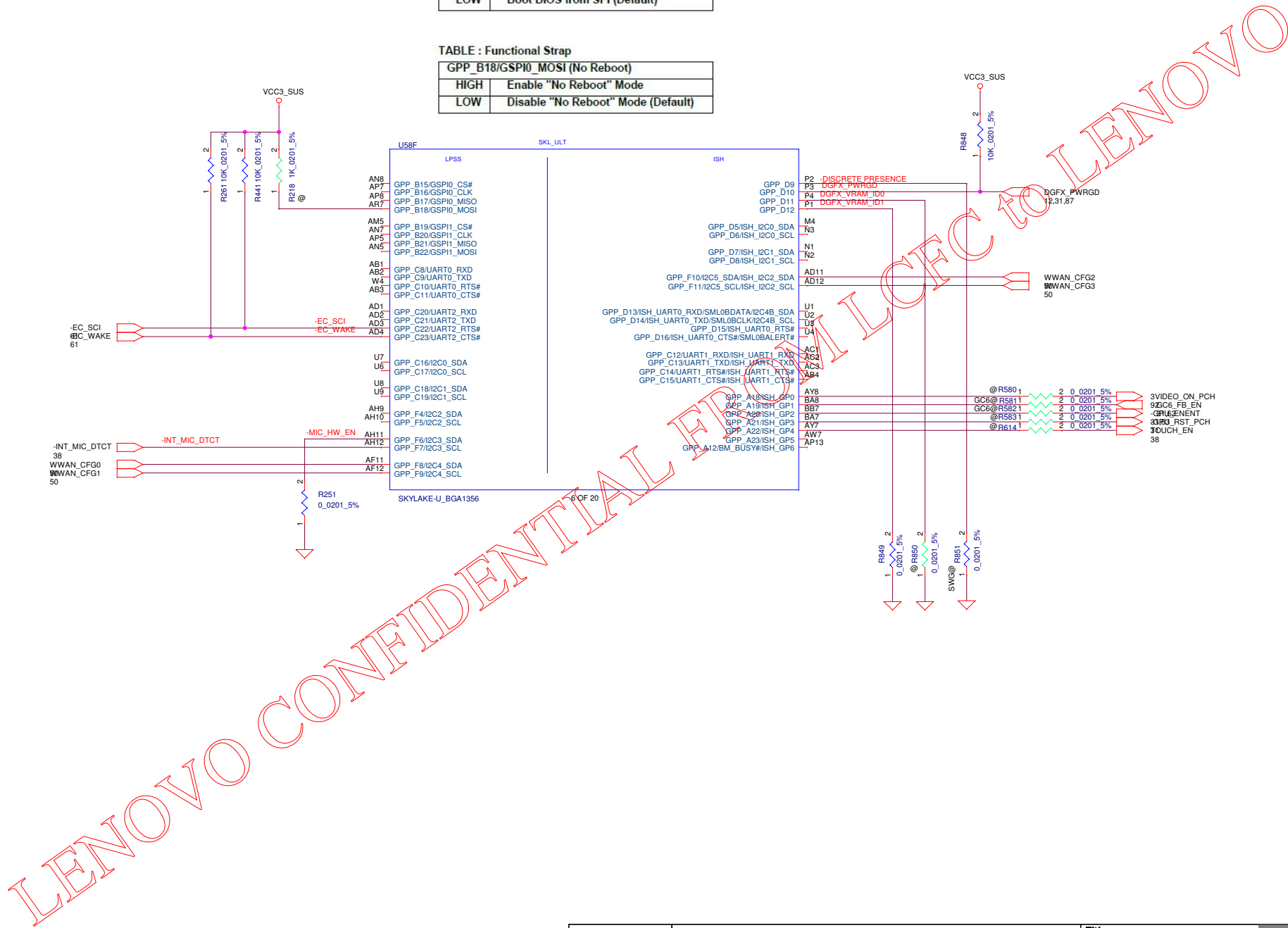
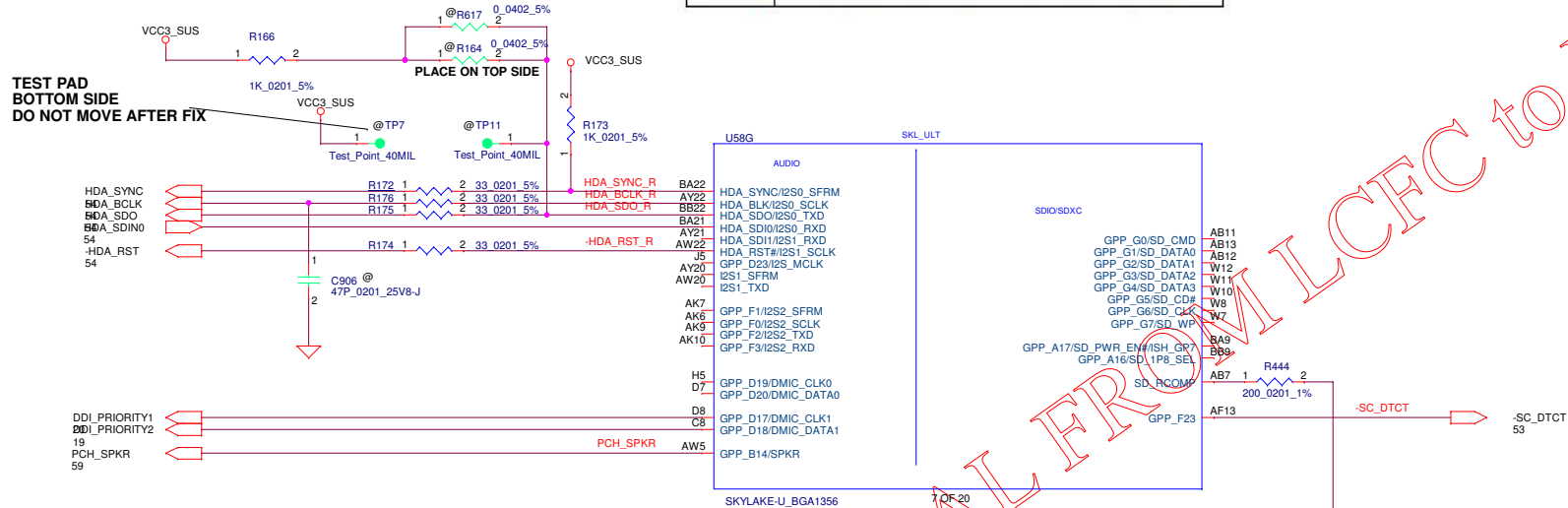




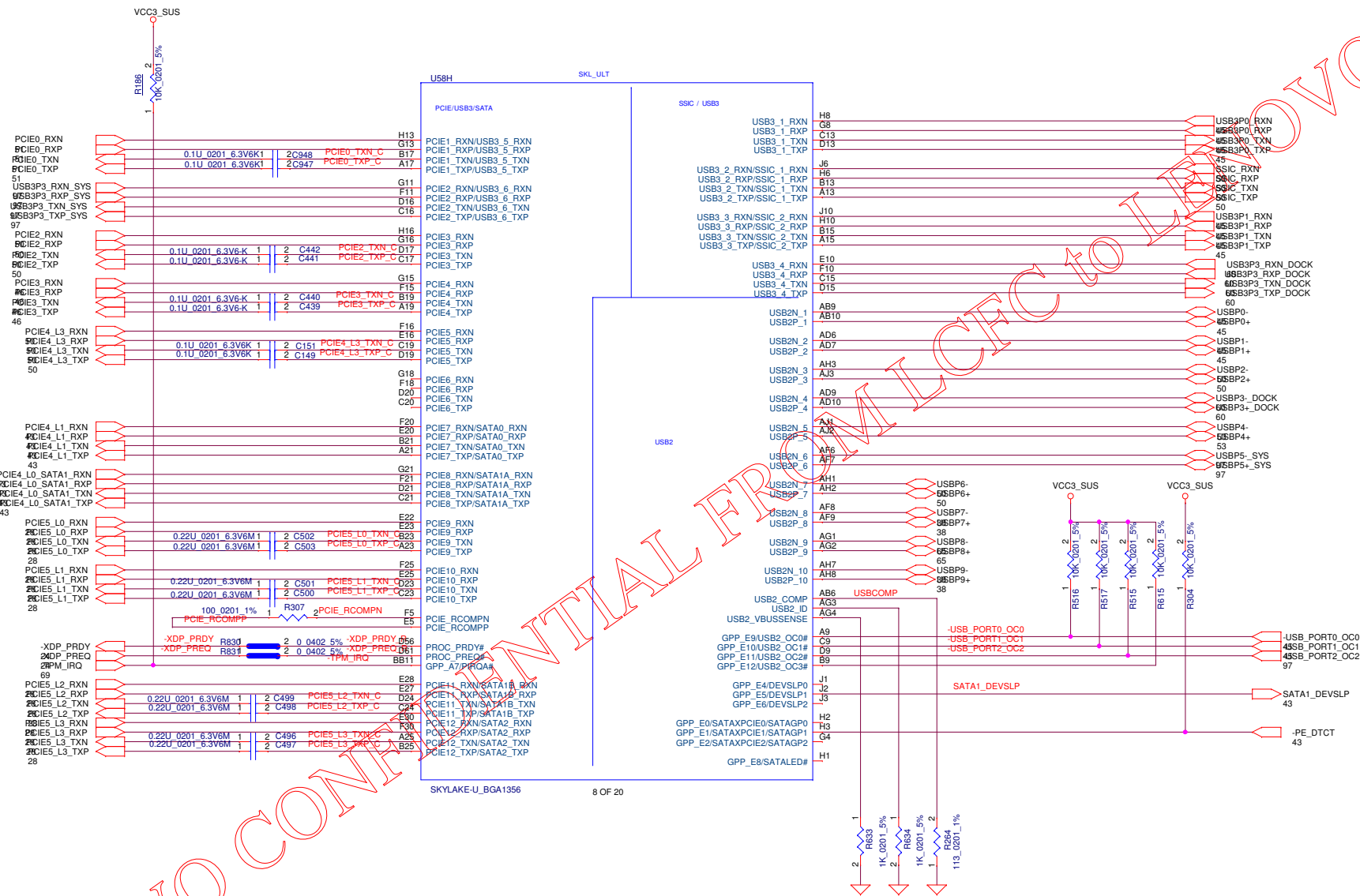
TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)



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Title		LCFC	
CPU(7/16) : AUDIO/SDXC			
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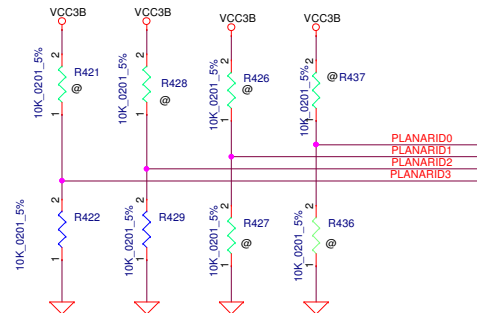
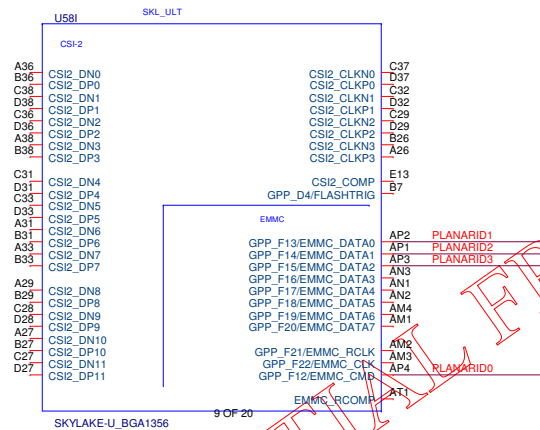
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Title		
CPU(8/16) : SYSTEM PM		
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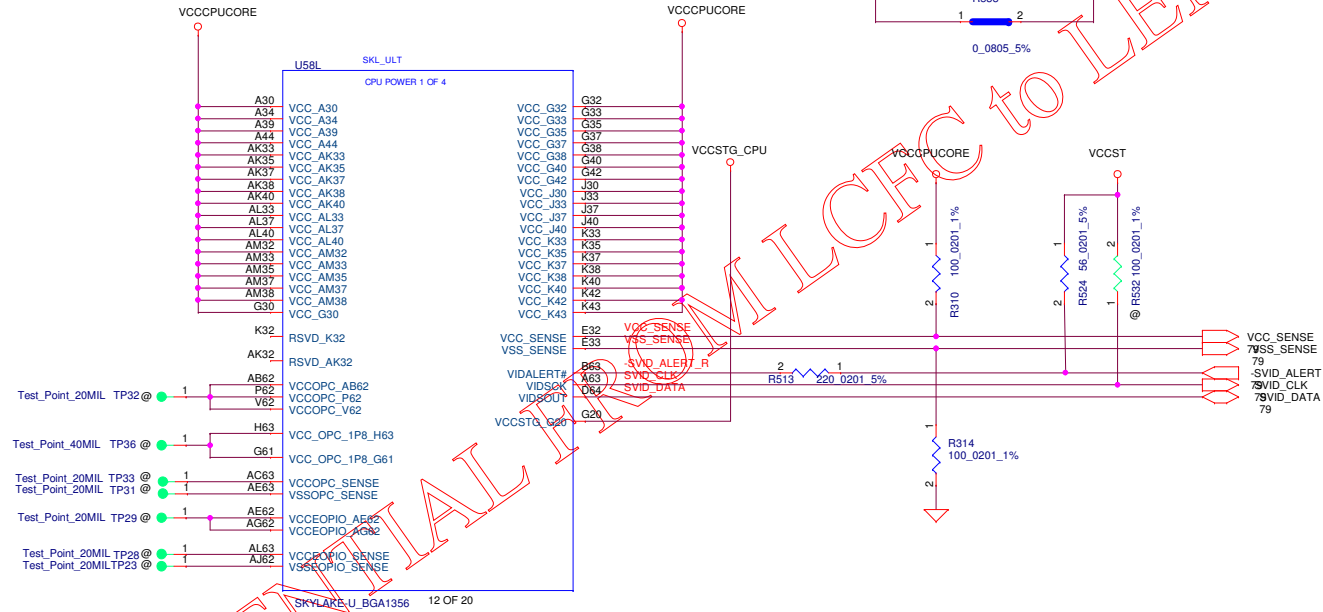
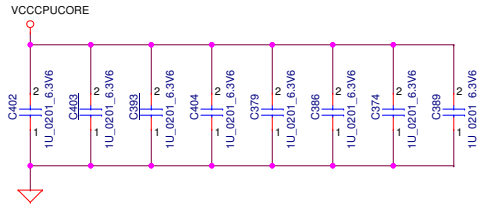
PLANAR ID TABLE		
LEVEL		PLANARID[3..0]
UMA	SWG	
SDV		0000B
FVT		0001B
SIT	FVT	0010B
SVT	SIT	0011B
	SVT	0100B

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Title			
CPU(9/16) : CSI-2/EMMC			
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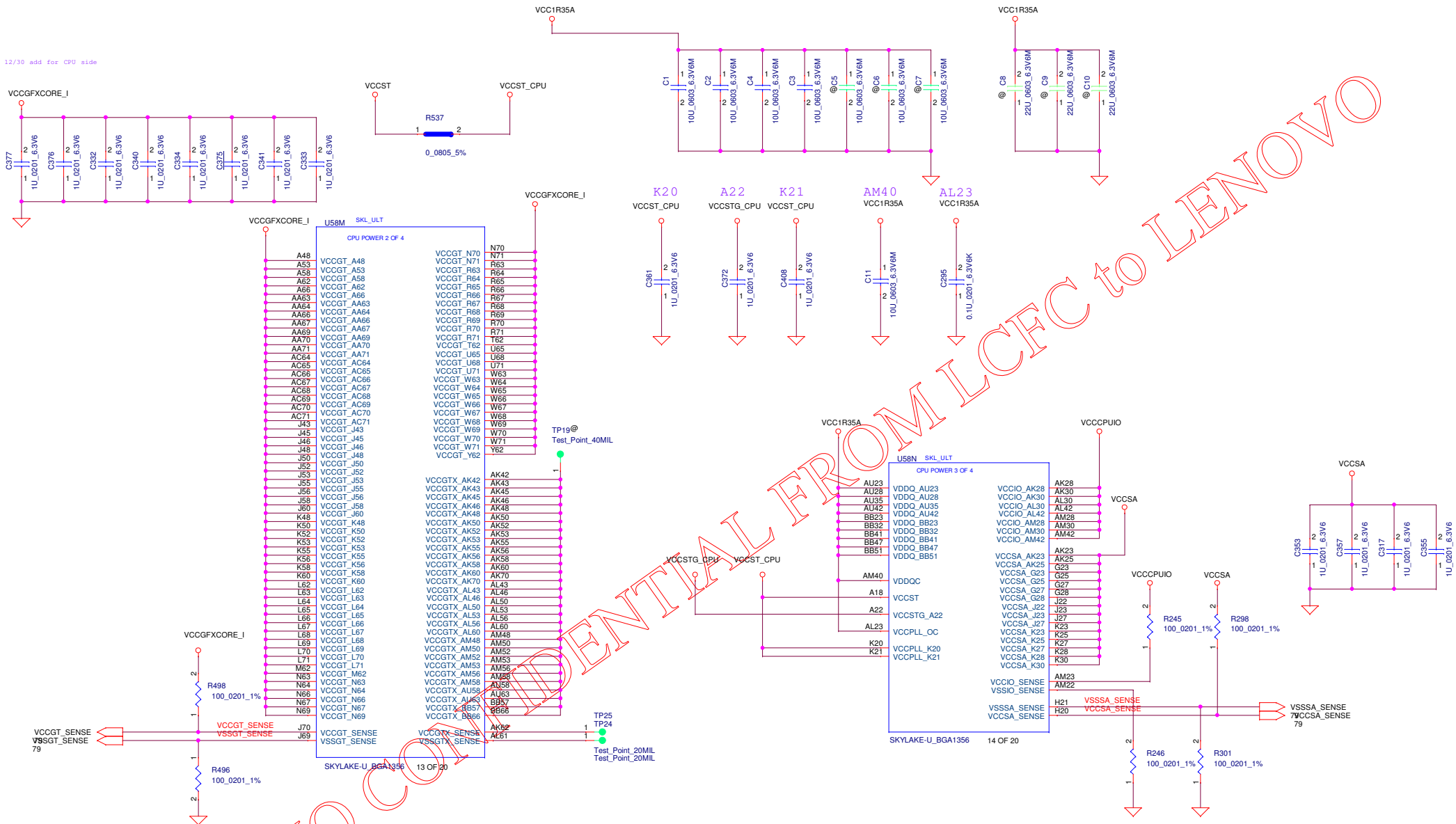




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12/30 add for CPU side

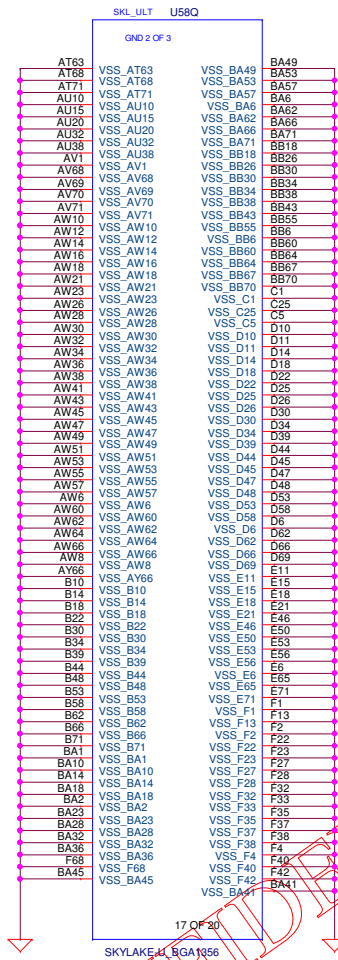
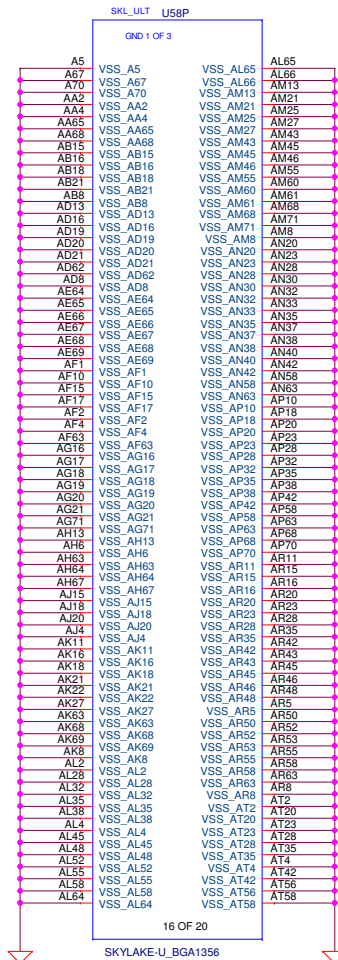


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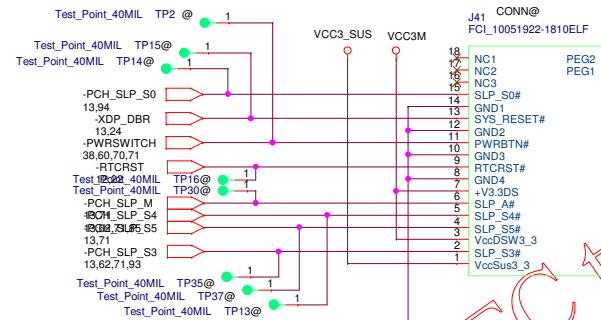
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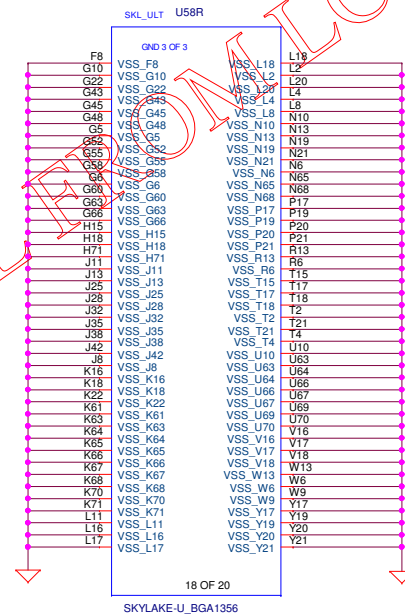




## APS/PETS interface

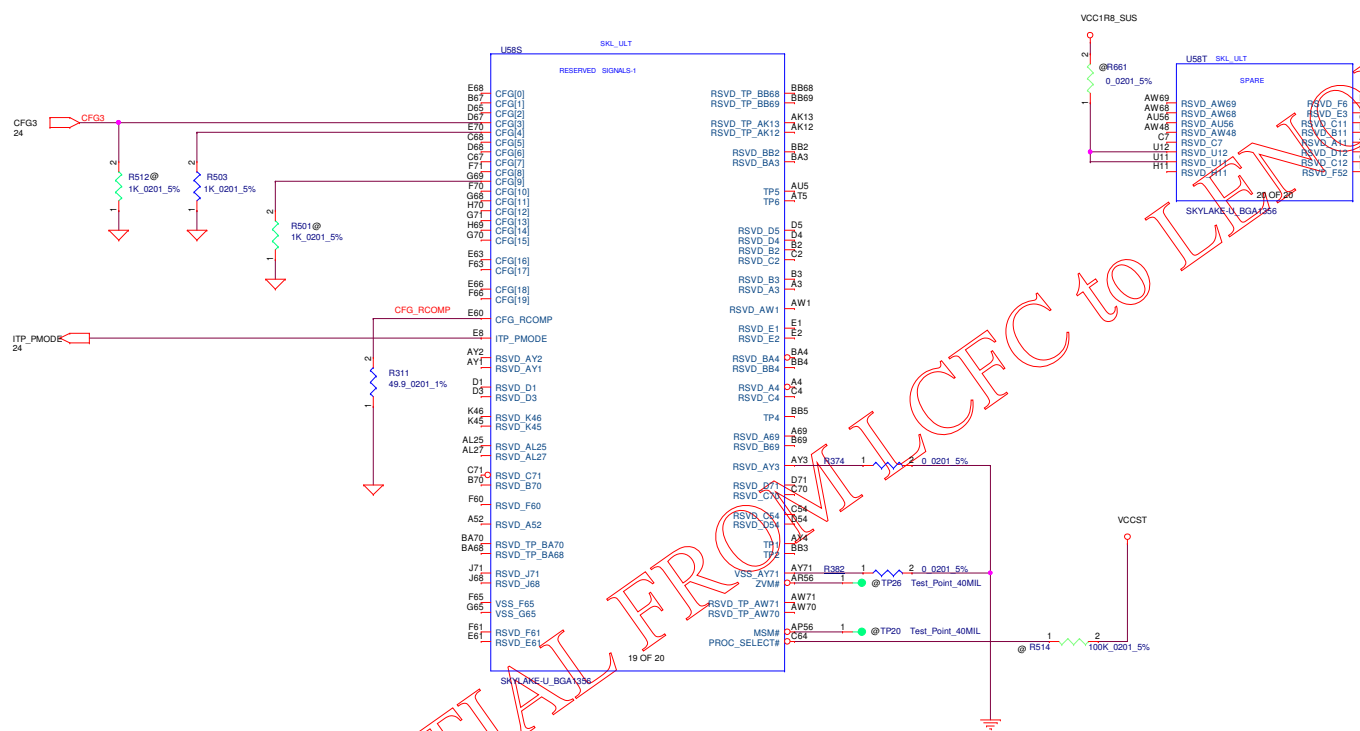


CONNECTOR	Planar Only	BOX
J41	ASM	NO ASM



TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled




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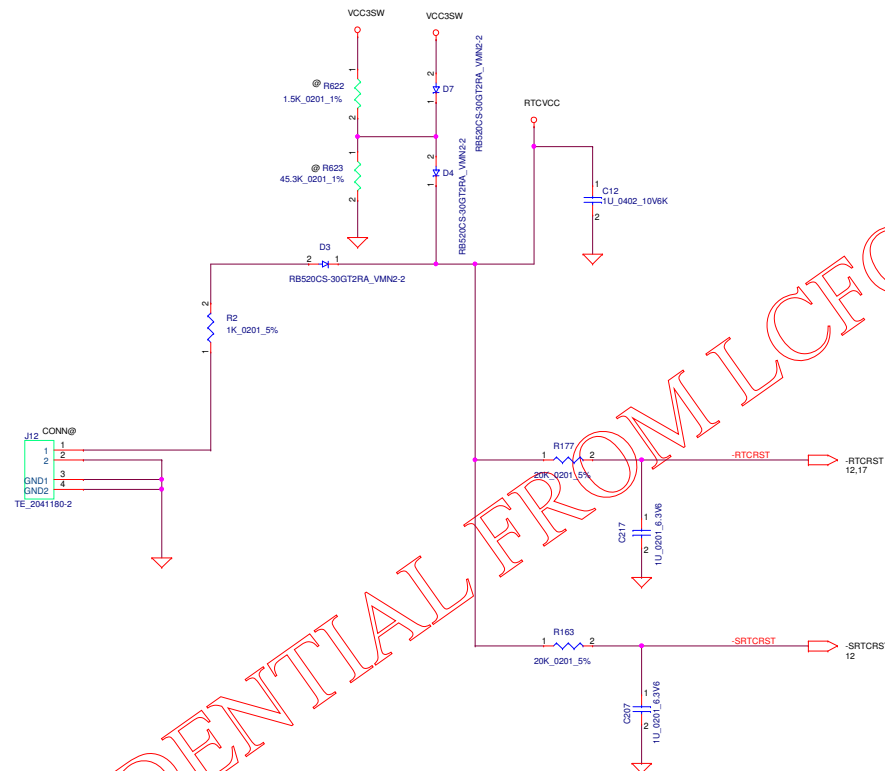


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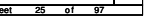


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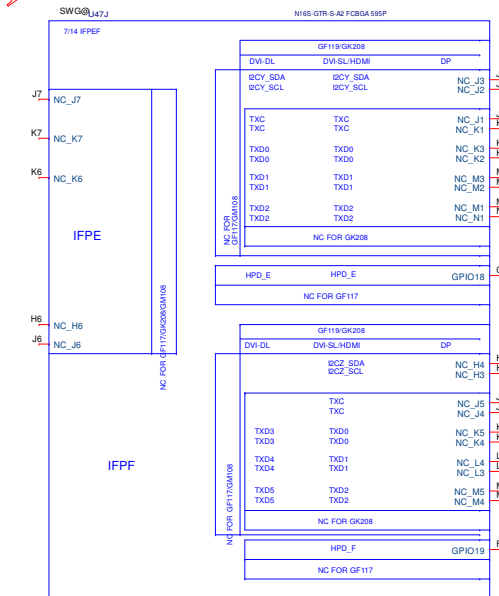
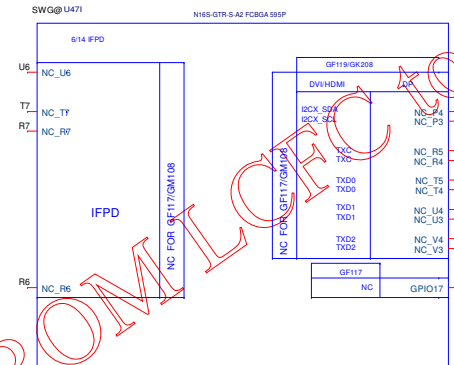
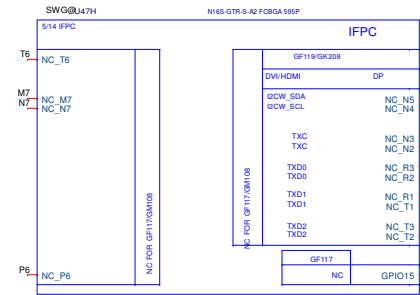
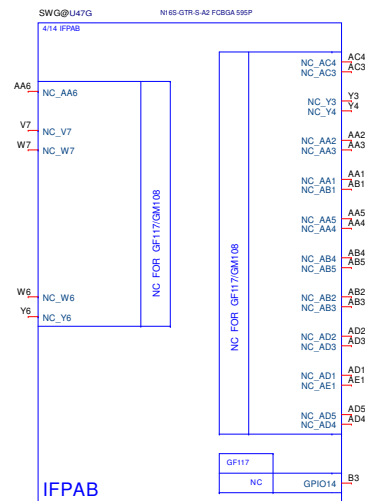


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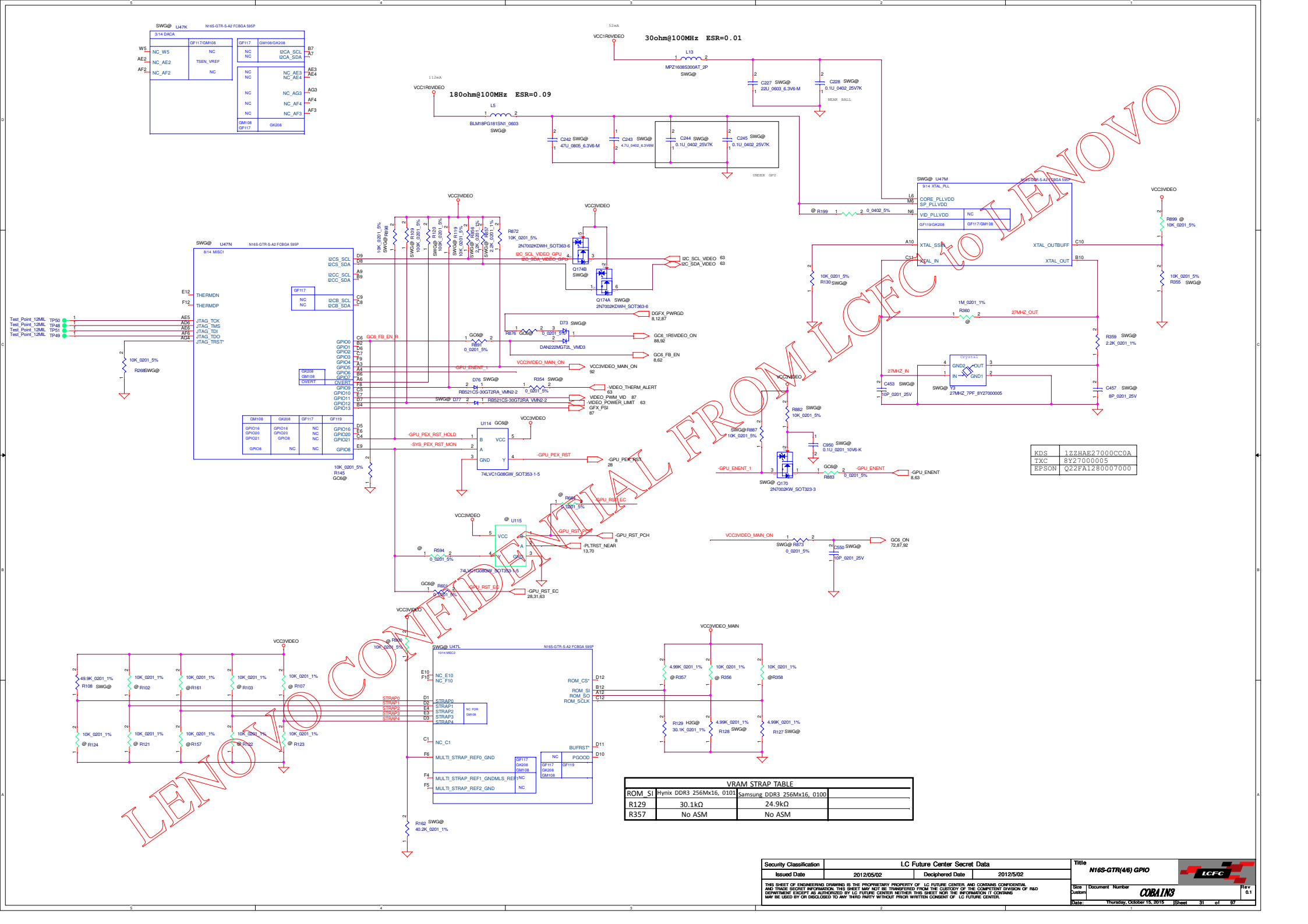
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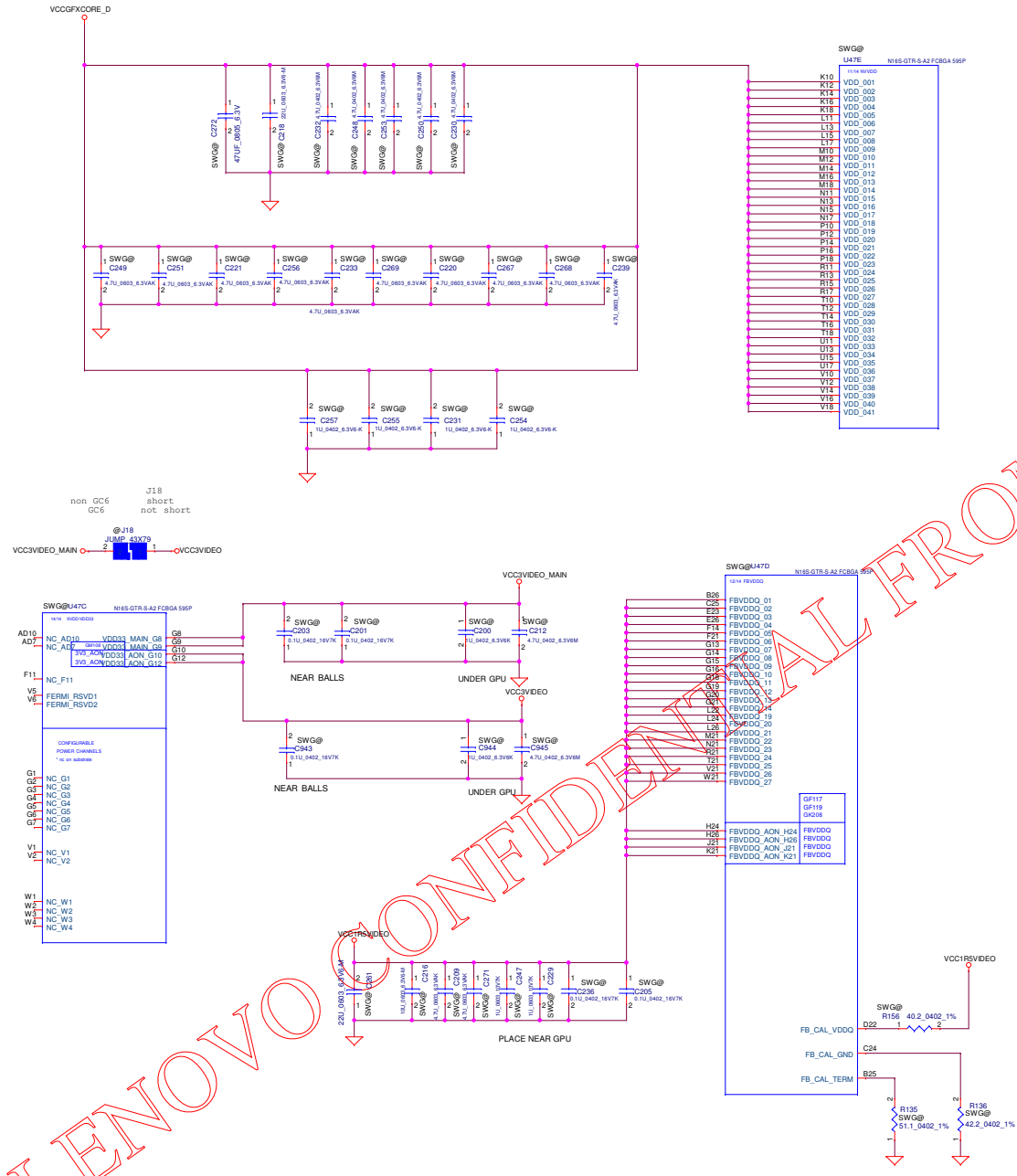




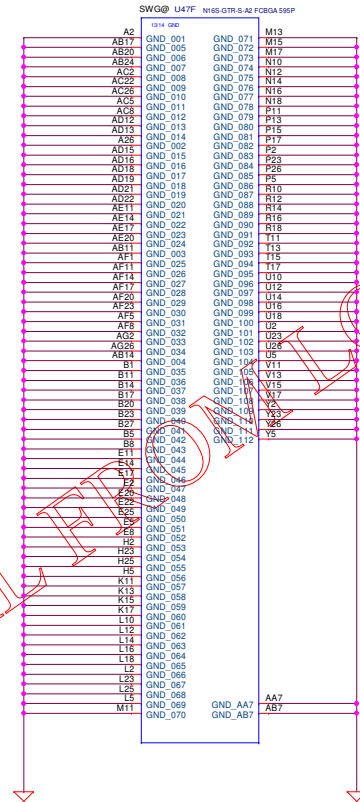


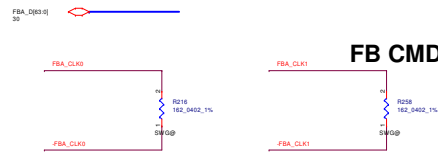
KDS	1ZZHAE27000CC0A
TXC	8Y27000005
EPSON	Q22FA1280007000

VRAM STRAP TABLE			
ROM SI	Hynix DDR3 256Mx16, 0101	Samsung DDR3 256Mx16, 0100	
R129	30.1kΩ	24.9kΩ	
R357	No ASM	No ASM	



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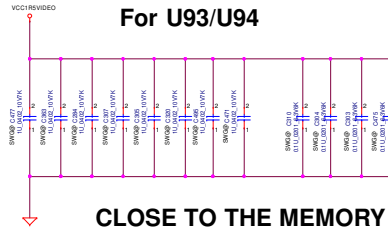
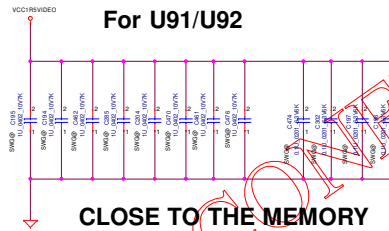
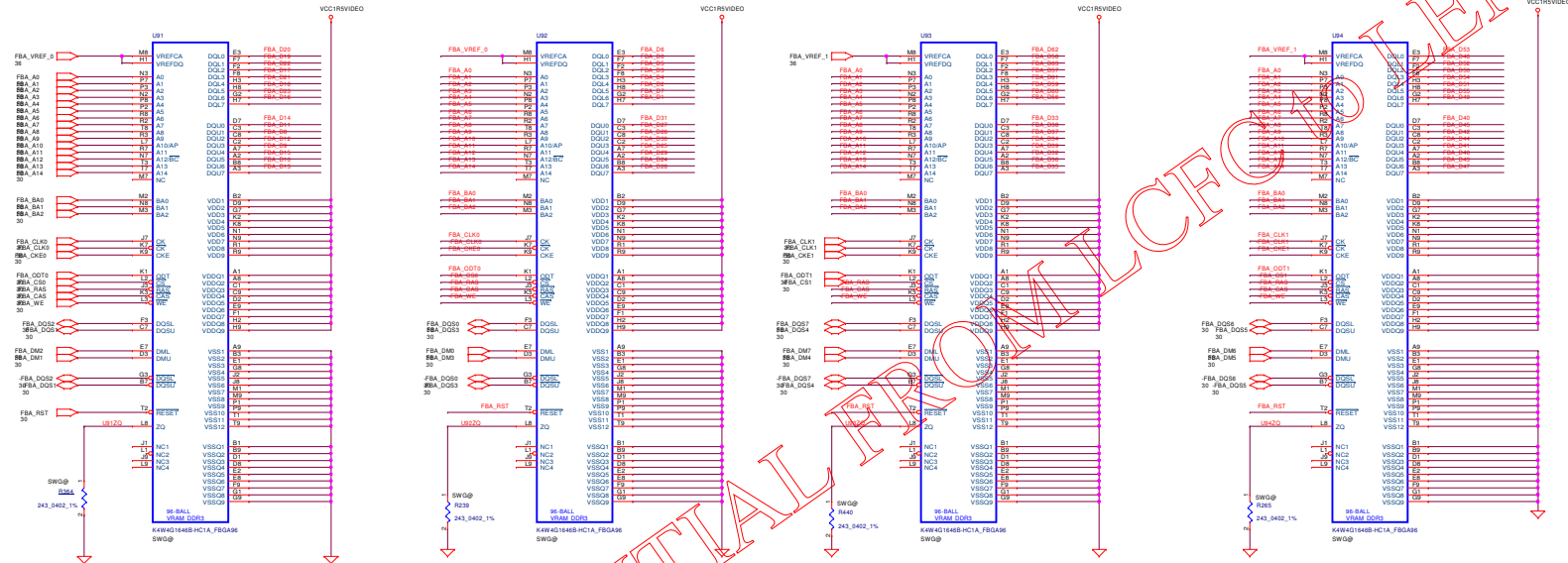




FB CMD mapping Mode D-N14x


TABLE D0R3 VIDEO MEMORY

	Micron 2GBITS (128Mx16)	HYNIX 2GBITS(128Mx16)	SAMSUNG 2GBITS(128Mx16)	SAMSUNG 4GBITS(256Mx16)	HYNIX 4GBITS(256Mx16)
U91 U92 U93 U94				K4W4G1646E-BC1A	H5TC4G63CFR-N0C
BOM Structure				S2G@	H2G@

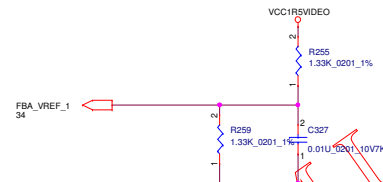
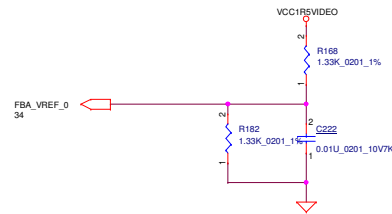


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				Date:	Thursday, October 15, 2015 15:58 37 of 87




Rev  
0.1



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				Document Number		0.1	
				Date:		Thursday, October 15, 2015 Sheet 99 of 97	

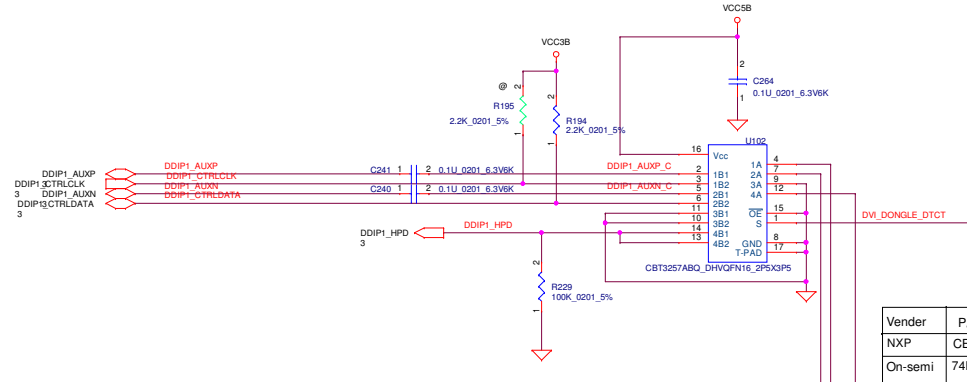
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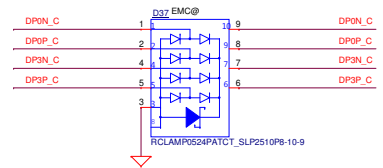
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				Quarter	COBAIN SWG
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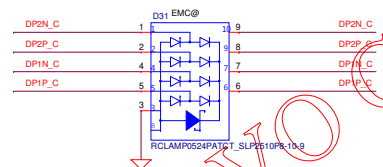
Rev 0.1



Vender	P/N
NXP	CBT3257ABQ
On-semi	74FST3257MNTWG



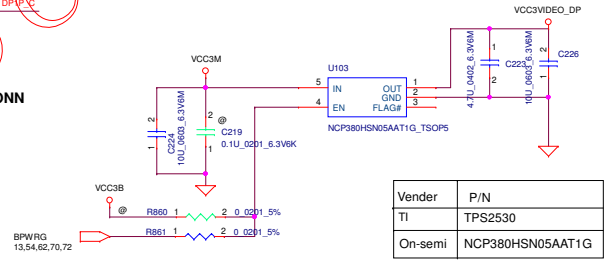
NEAR DP CONN



NEAR DP CONN

NEAR DP CONN

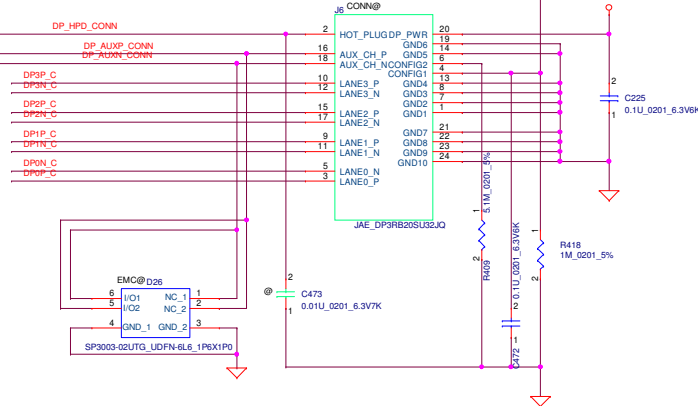
Typ. 500mA  
Max 1.5A



Vender	P/N
TI	TPS2530
On-semi	NCP380HSN05AAT1G

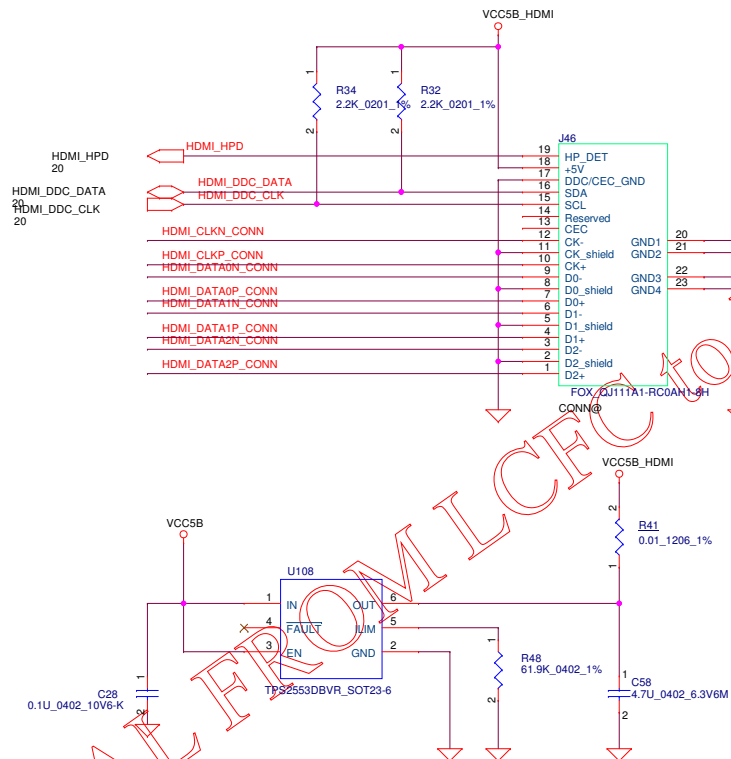
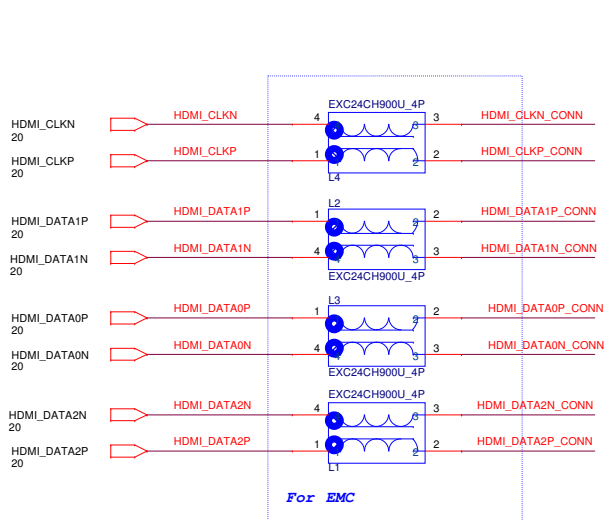
DDIP1_3V	C315 1	2	0.1U 0201 6.3V6K	DP3N_C
DDIP1_2P	C319 1	2	0.1U 0201 6.3V6K	DP3P_C
DDIP1_2N	C263 1	2	0.1U 0201 6.3V6K	DP2N_C
DDIP1_2P	C265 1	2	0.1U 0201 6.3V6K	DP2P_C
DDIP1_1N	C266 1	2	0.1U 0201 6.3V6K	DP1N_C
DDIP1_1P	C276 1	2	0.1U 0201 6.3V6K	DP1P_C
DDIP1_0N	C280 1	2	0.1U 0201 6.3V6K	DP0N_C
DDIP1_0P	C284 1	2	0.1U 0201 6.3V6K	DP0P_C

### DP CONN

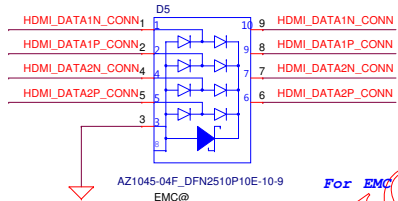


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Deciphered Date	2012/06/21

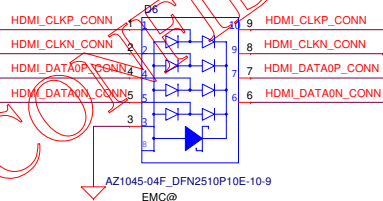
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41	COBAIN SWG	0.1
Date:	Thursday, October 18, 2012	Sheet 41 of 97



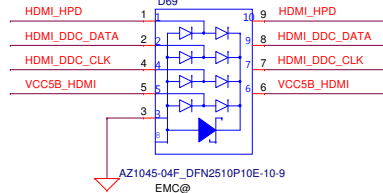
Close to J46



For EMC



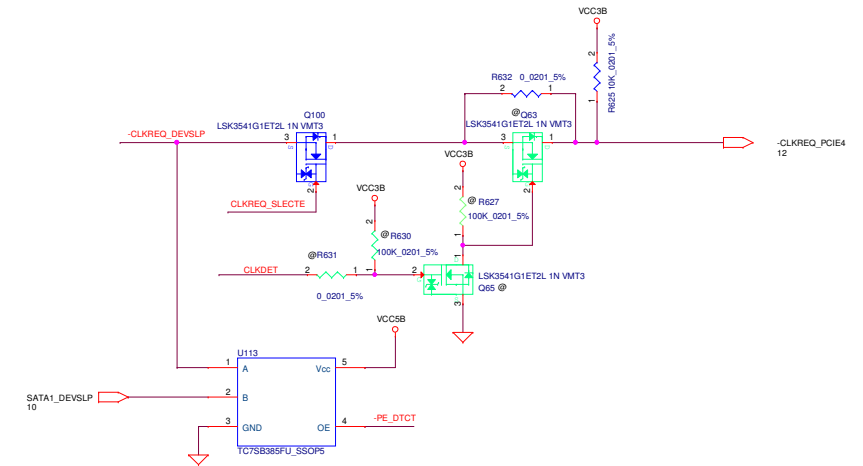
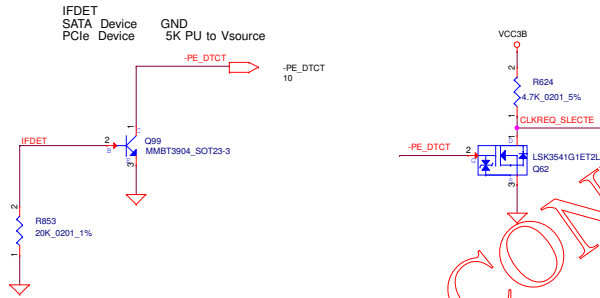
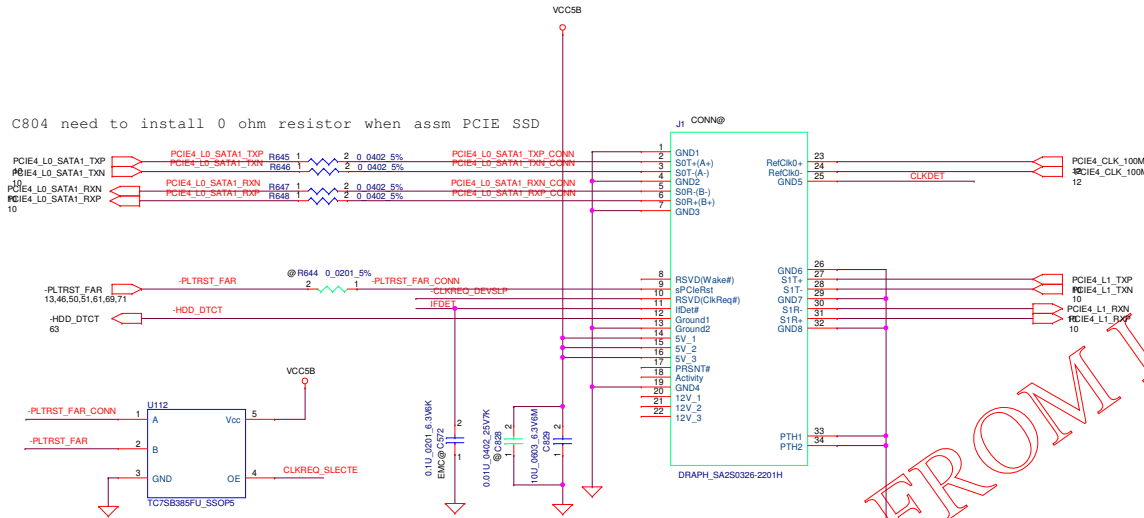
1/29 Add for RMI request



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Title		
HDMI CONN		
Size	Document Number	Rev
Custom	COBA1N3	0.1
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C803 and C804 need to install 0 ohm resistor when assm PCIe SSD



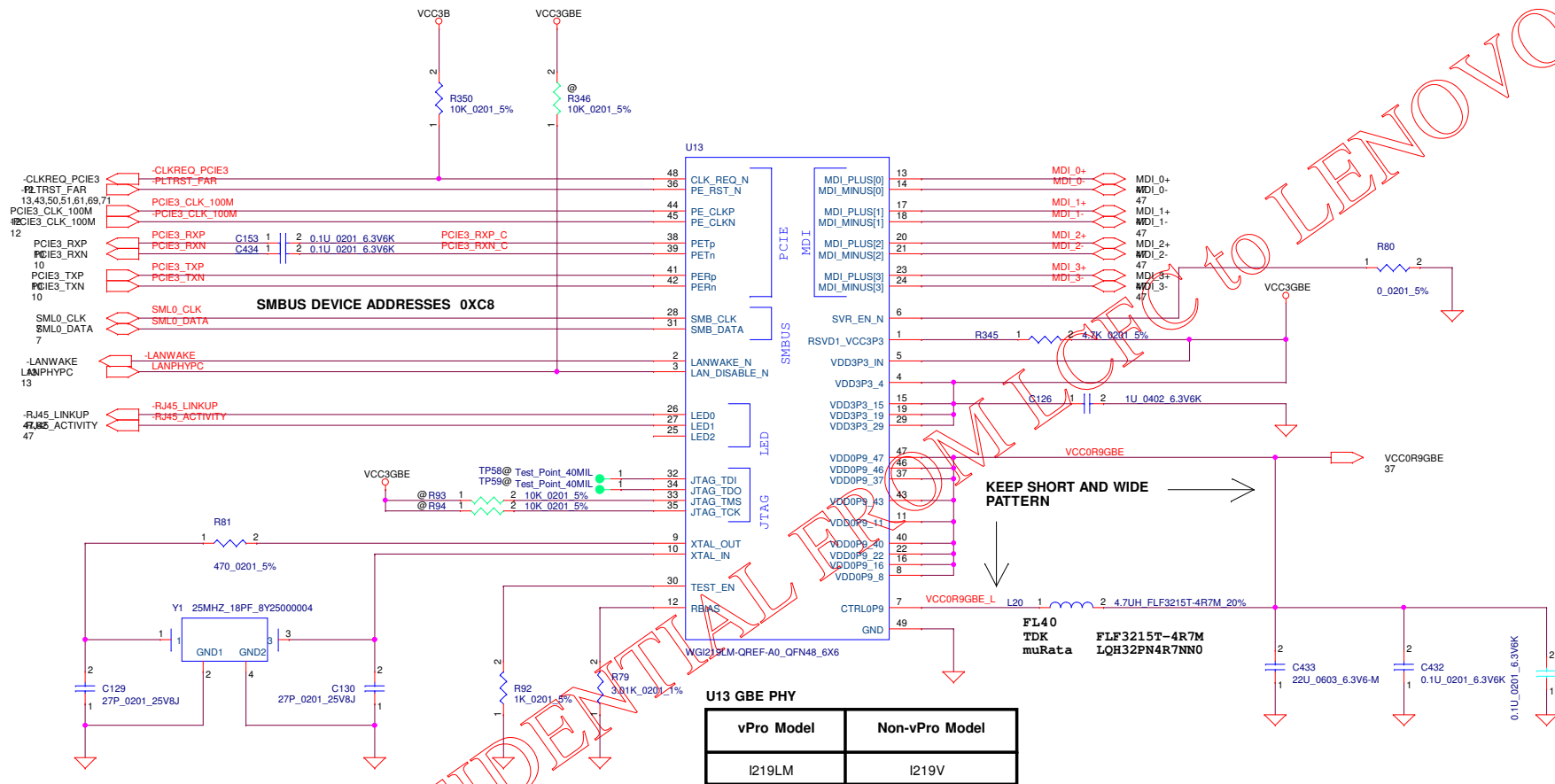
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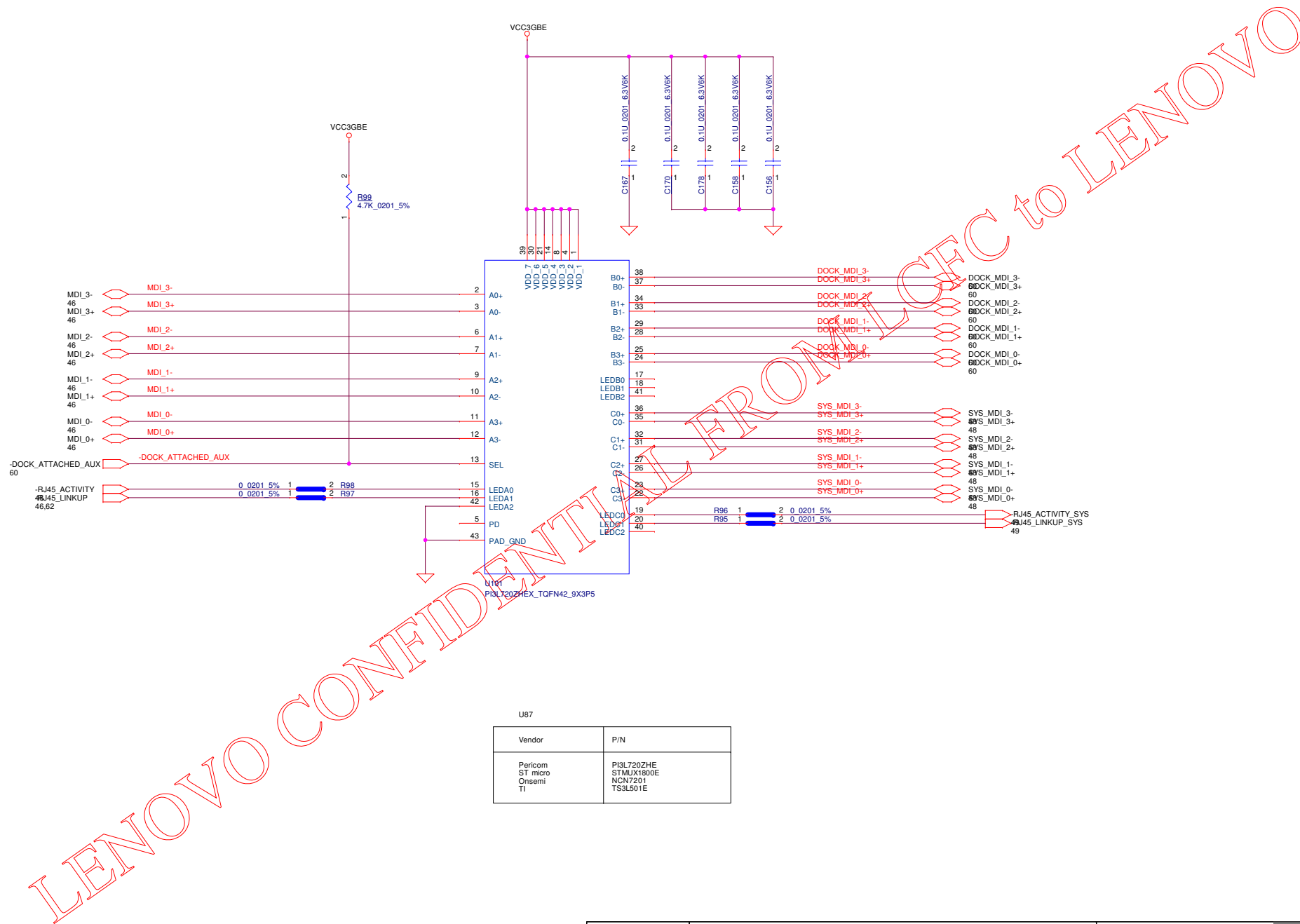
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Custom					0.1
Date:		Thursday, October 15, 2015 Sheet 44 of 97			







KDS 1ZZHAE25000CC0A  
 TXC 8Y25000004  
 EPSON Q22FA1280023800



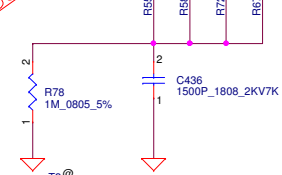
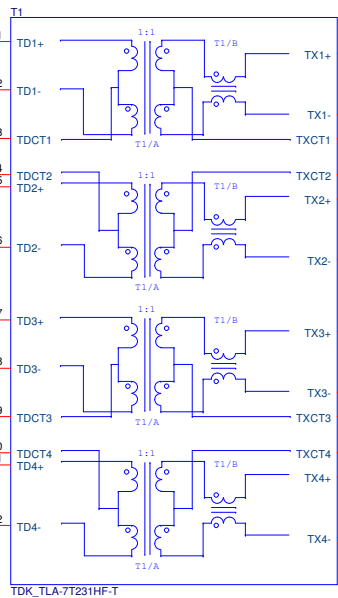
U87	
Vendor	P/N
Pericom ST micro Onsemi TI	PIC1720ZHE STMUX1800E NCH7201 TS3L501E

THE WIDTH OF THESE TRACE SHOULD BE WIDER THAN 35MIL TO PREVENT VOLTAGE DROP.

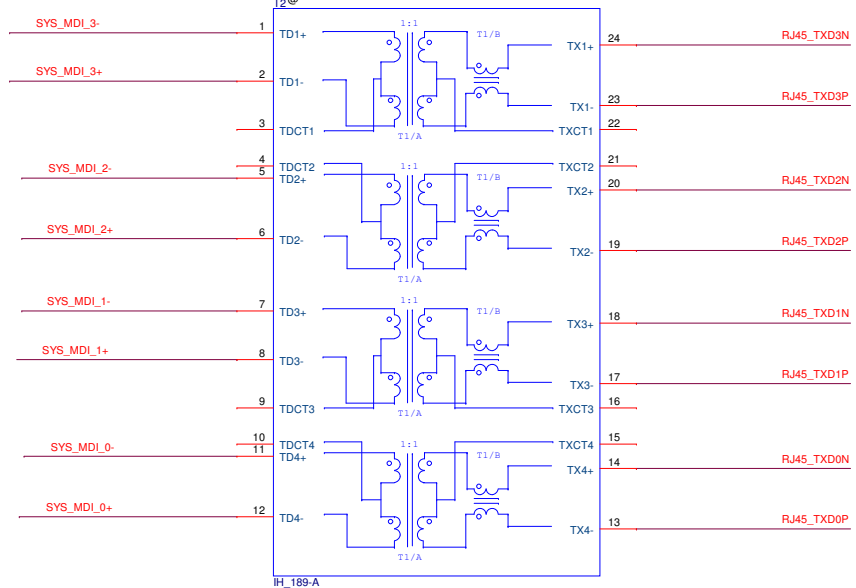
C303 SHOULD BE PLACED AS CLOSE TO MAGNETICS AS POSSIBLE.

ESD REASON

Vendor	P/N
TDK	TLA-7T231HF-T
Timag	IH-115-F
Bothand	NA69LF



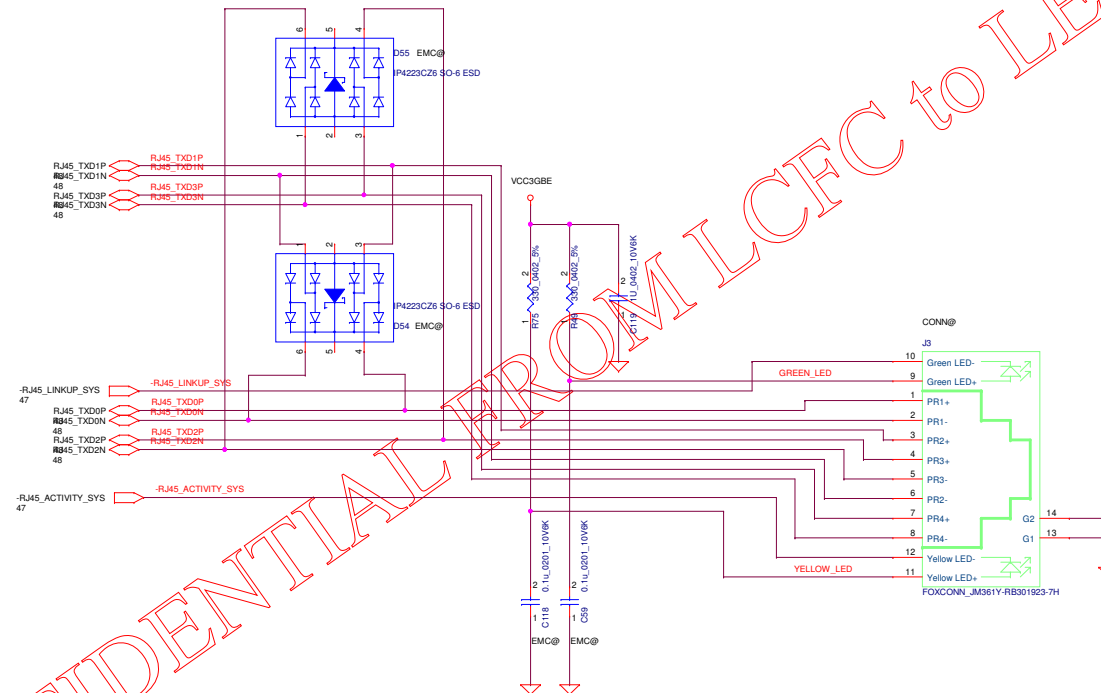
PATTERN MUST BE SHORT AND WIDE.  
HIGH VOLTAGE  
1500PF CAP  
IS OPTIONAL




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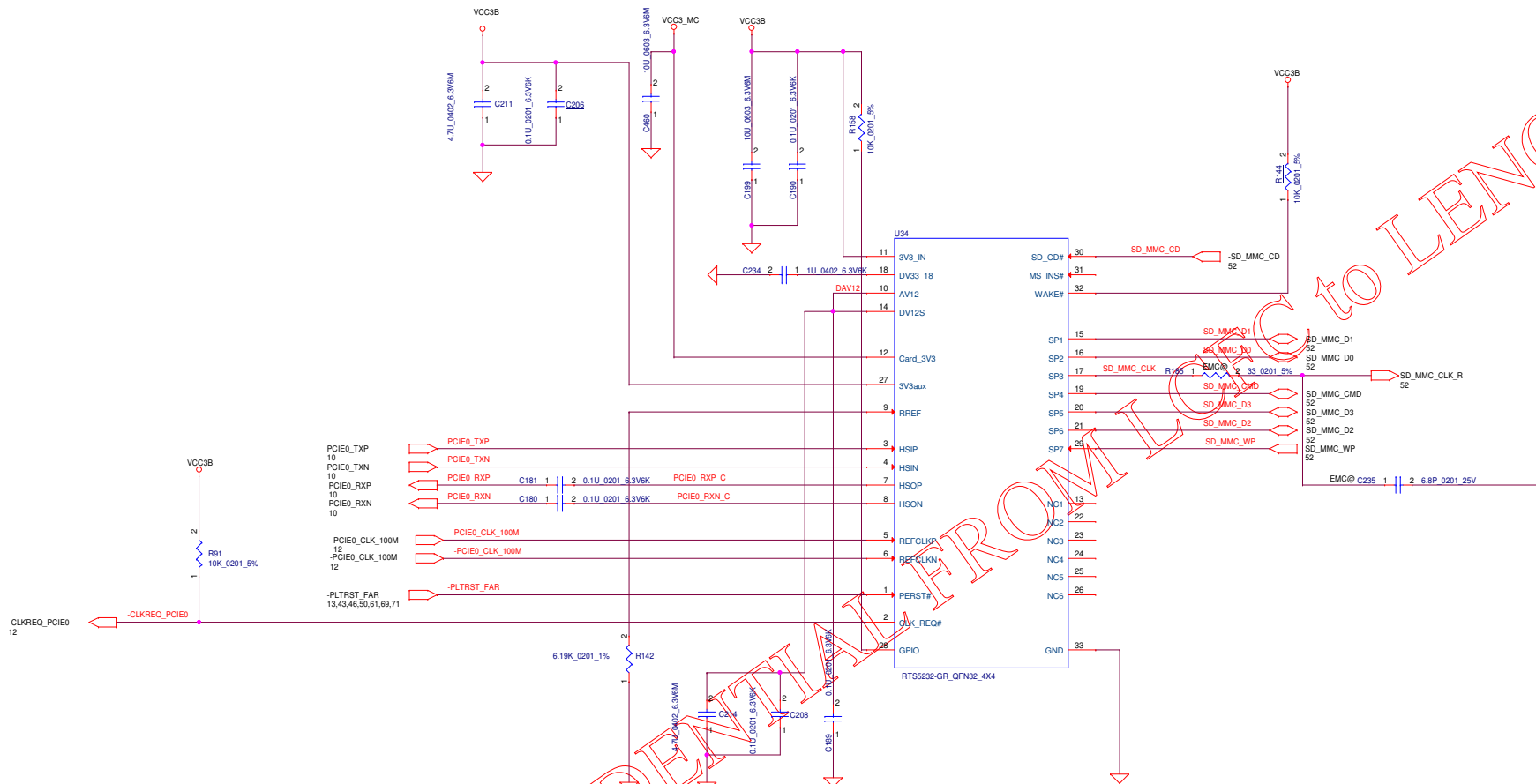
GBE MAGNETICS			Rev
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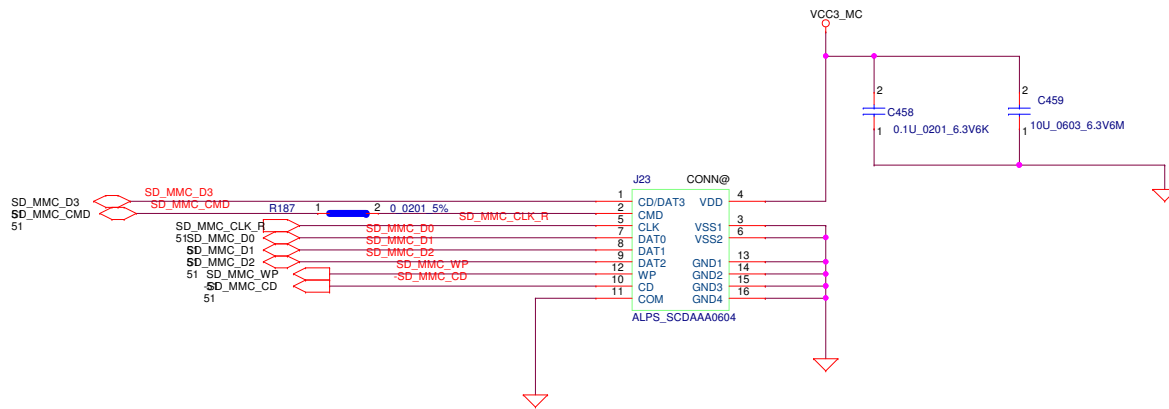
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Size			Document Number			COBAIN SWG		
Date:			Thursday, October 15, 2015			Sheet 49 of 97		





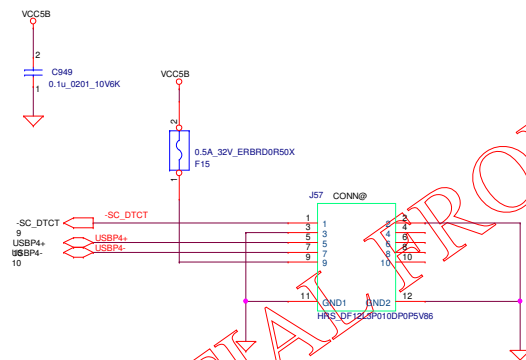


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				Date:	Thursday, October 15, 2015	Sheet	52 of 97



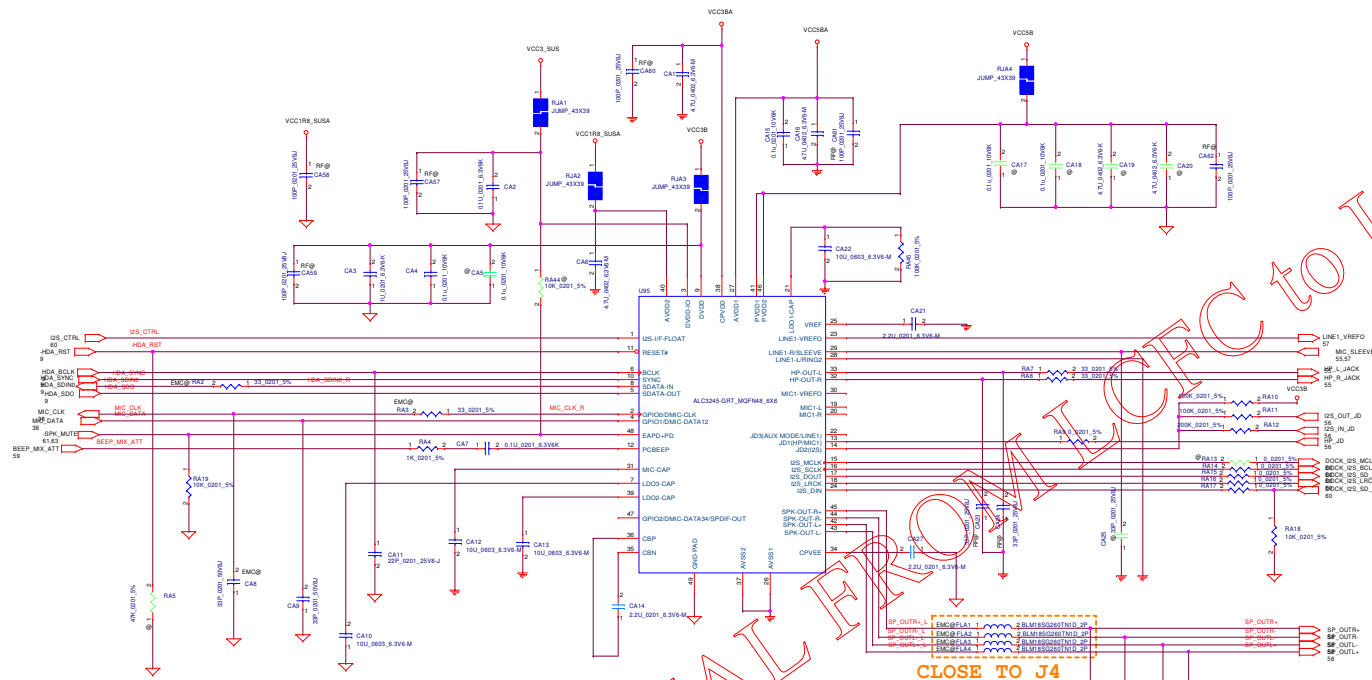
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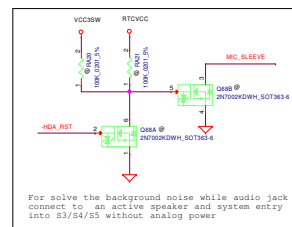


CORAINS

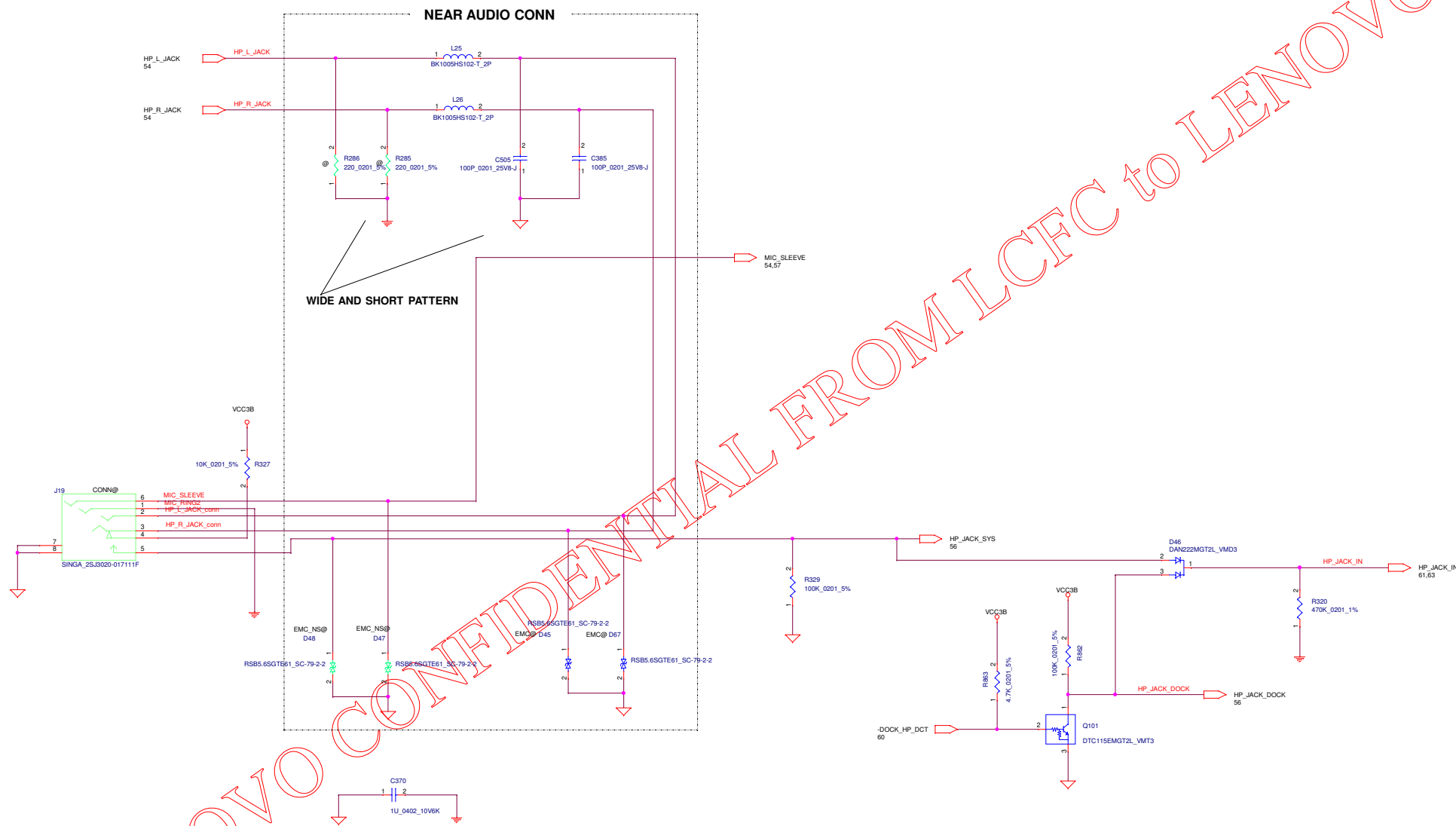


CLOSE TO J4

PLACE UNDER CODEC



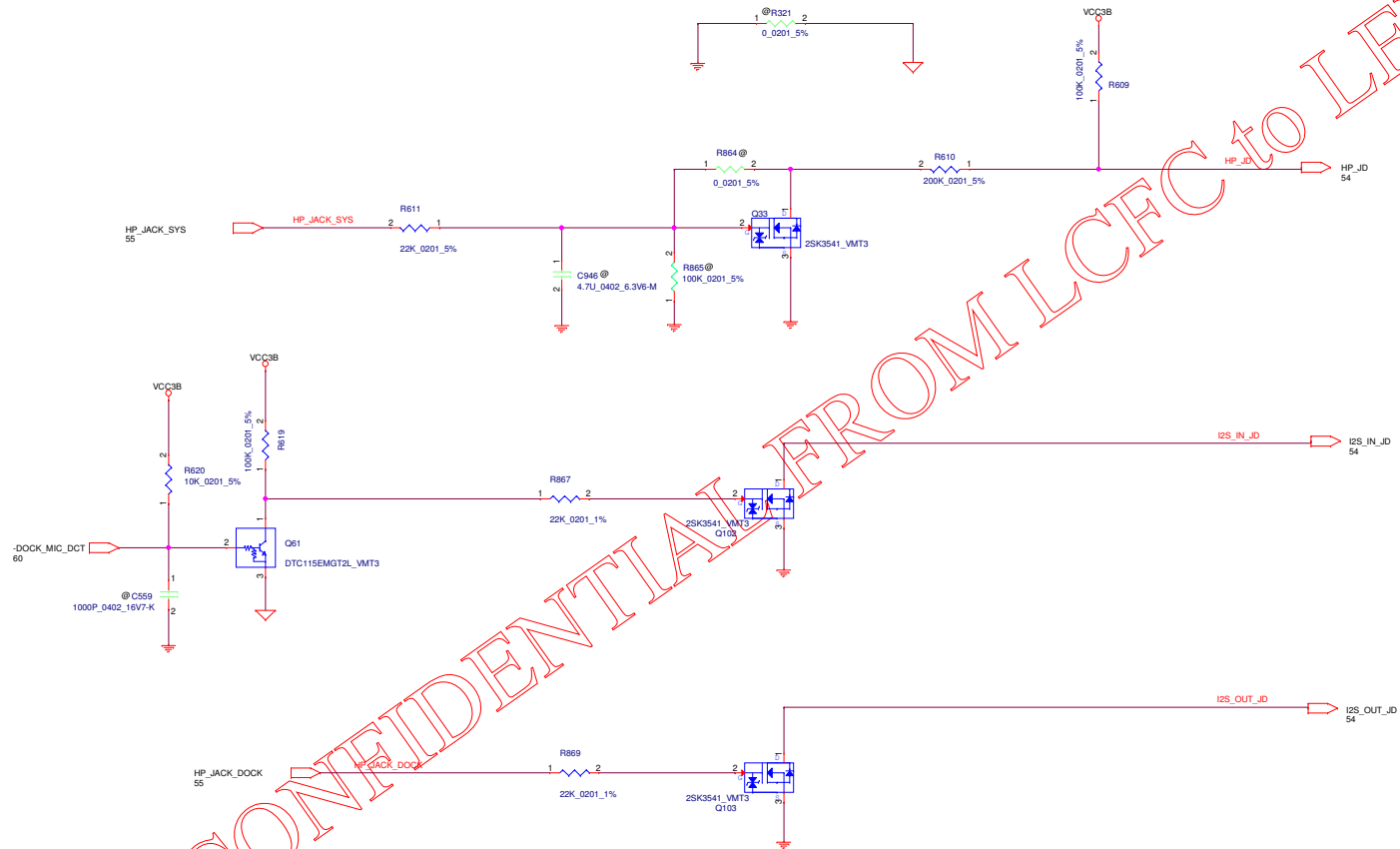
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Drawn	Wang, Chong	Reviewed	Wang, Chong	Checked	Wang, Chong



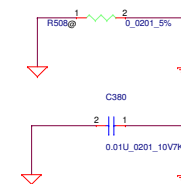
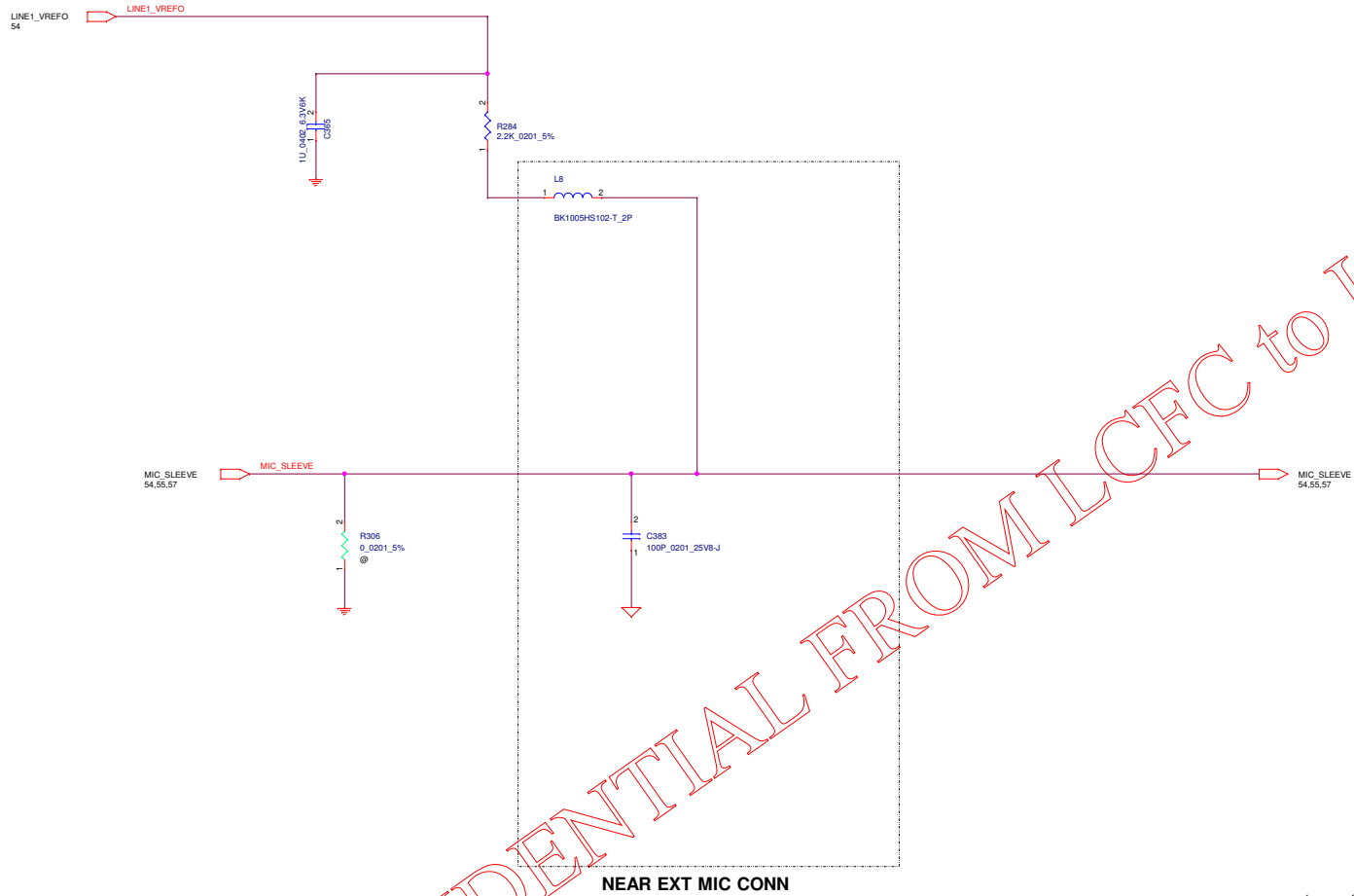
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Issued Date	2012/05/02	Deciphered Date	2012/5/02	AUDIO CONNECTOR	
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Custom					0.1
Date:		Thursday, October 15, 2015		Sheet	55 of 97



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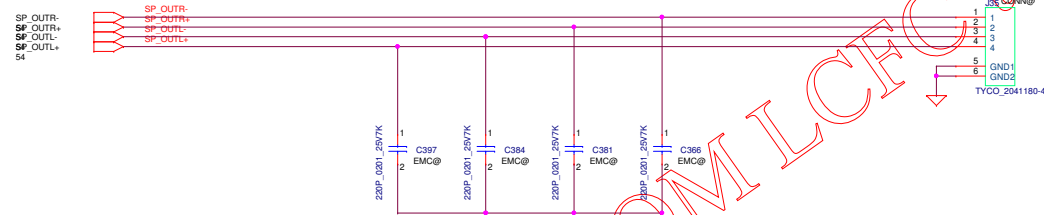


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2012/05/02		2012/5/02		Size	
Custom		C		Document Number	
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				Thursday, October 16, 2015	
				Sheet	
				56 of 97	



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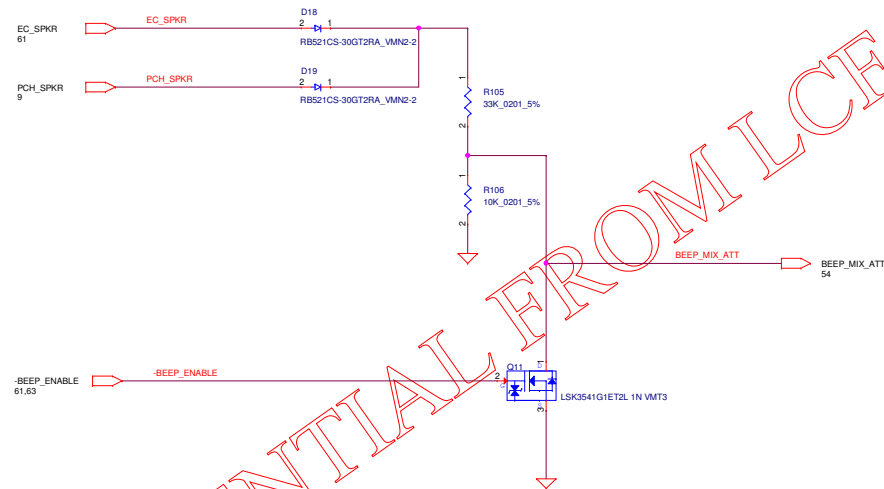
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Size	Document Number	Rev				
Date:		0.1				
Date: Thursday, October 15, 2015		Sheet	97	of 97		



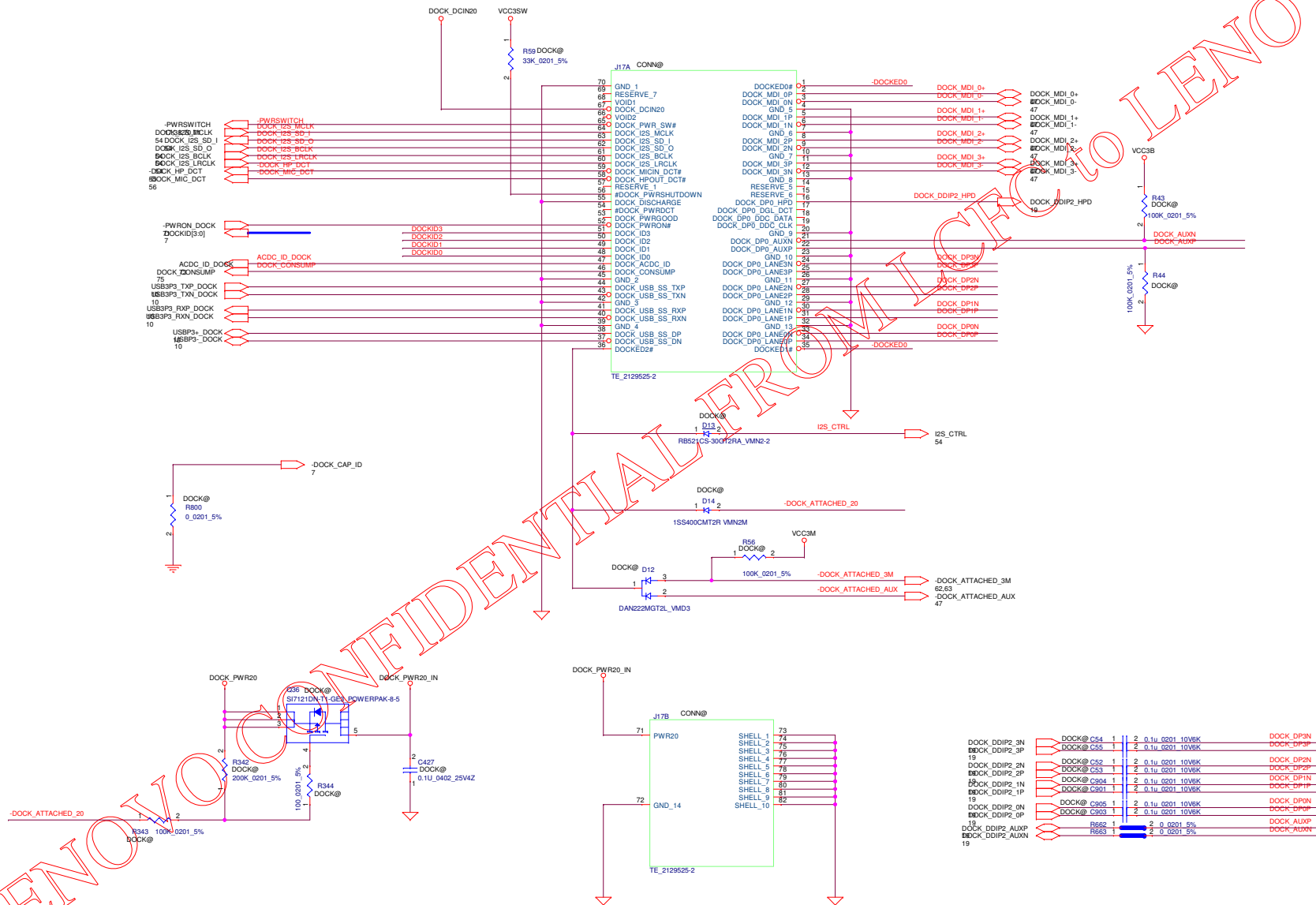
PLACE, NEAR SPEAKER CONNECTOR

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Issued Date		2012/05/02	Deciphered Date	2012/5/02	AUDIO SPEAKER
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Size	Document Number	COBAIN SWG		Rev	0.1
Custom		Thursday, October 15, 2015		Sheet	58 of 97

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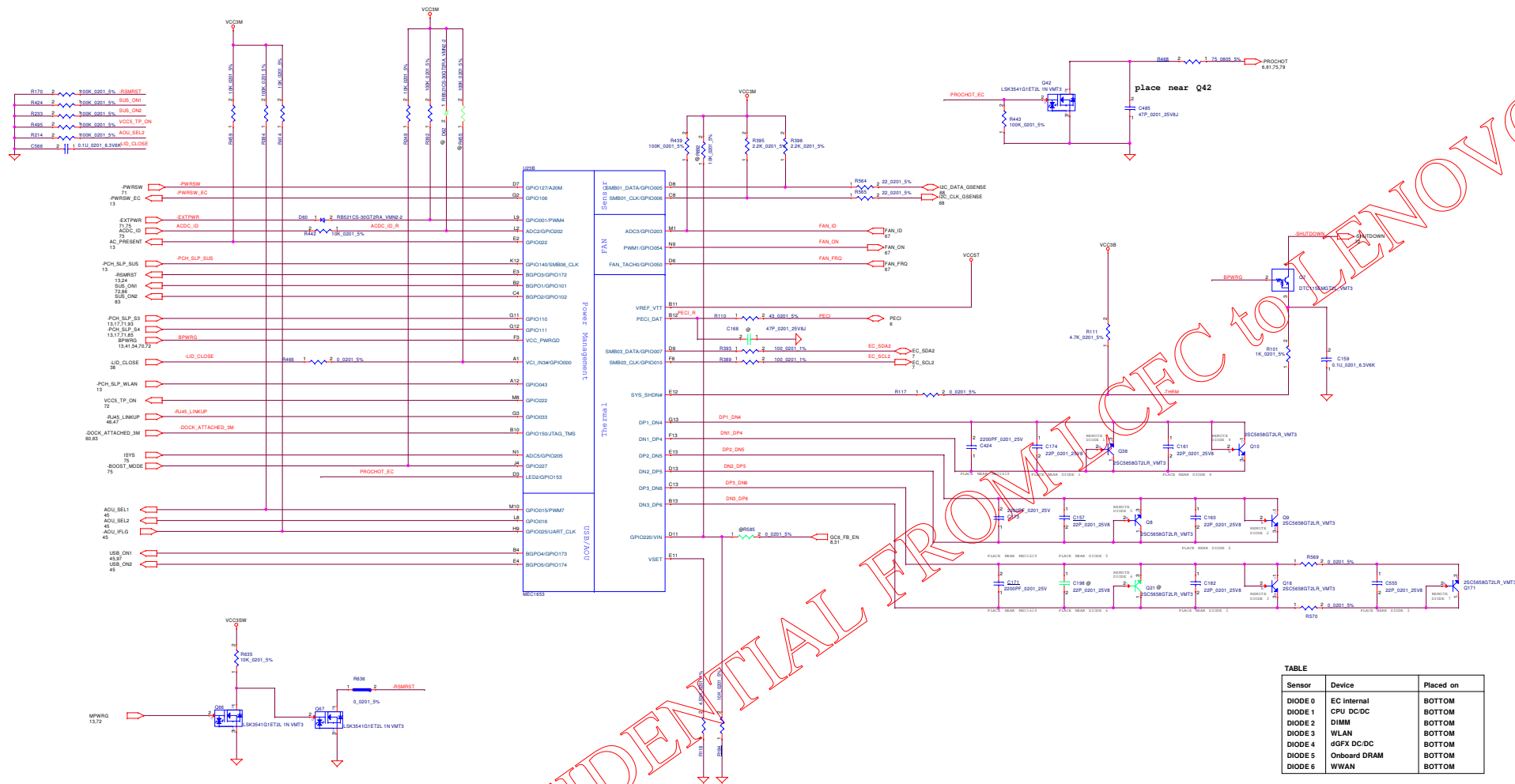


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Size	Document Number	COBAIN SWG		Rev	0.1
Custom		Thursday, October 15, 2015		Sheet	59 of 97



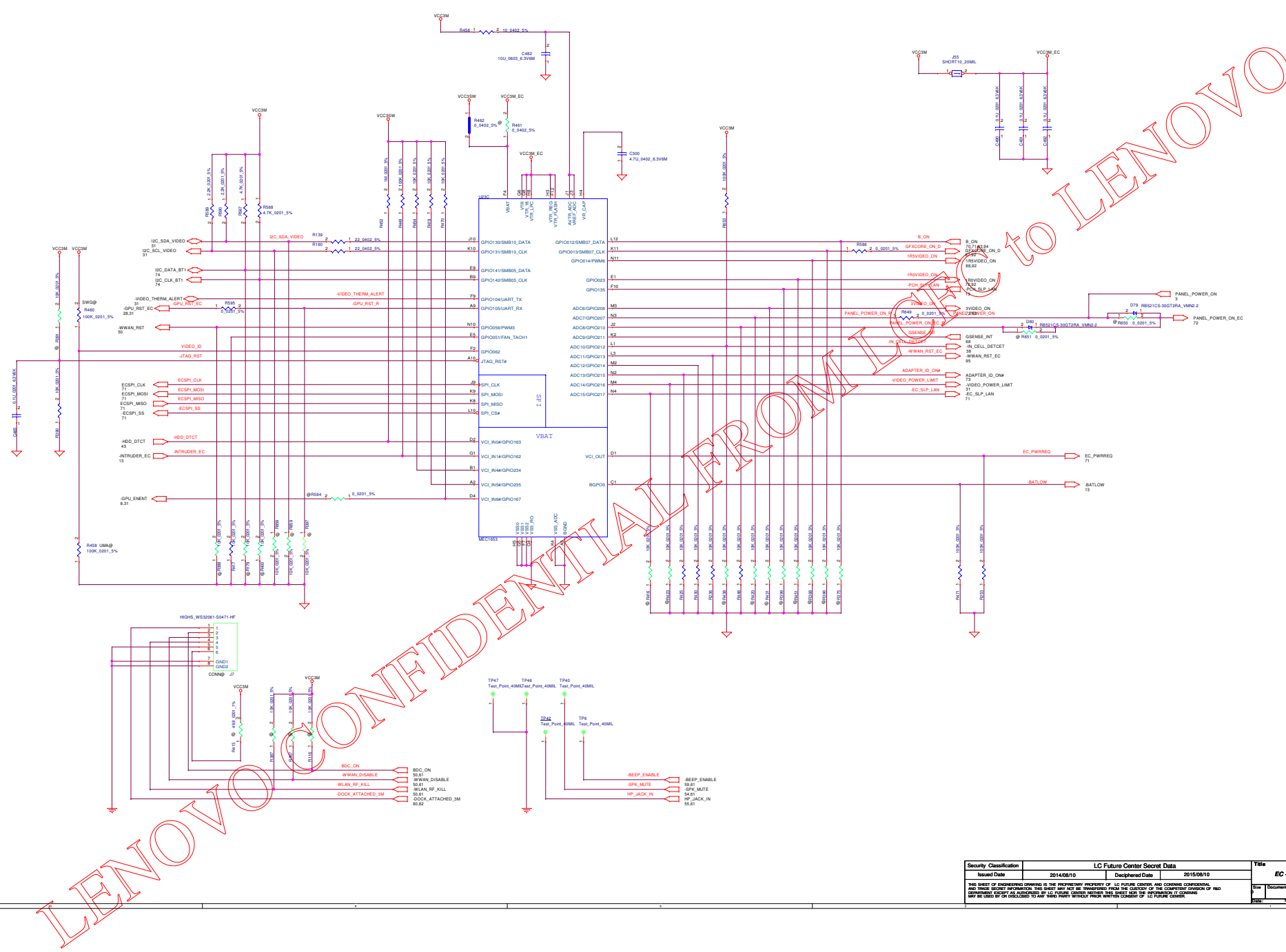




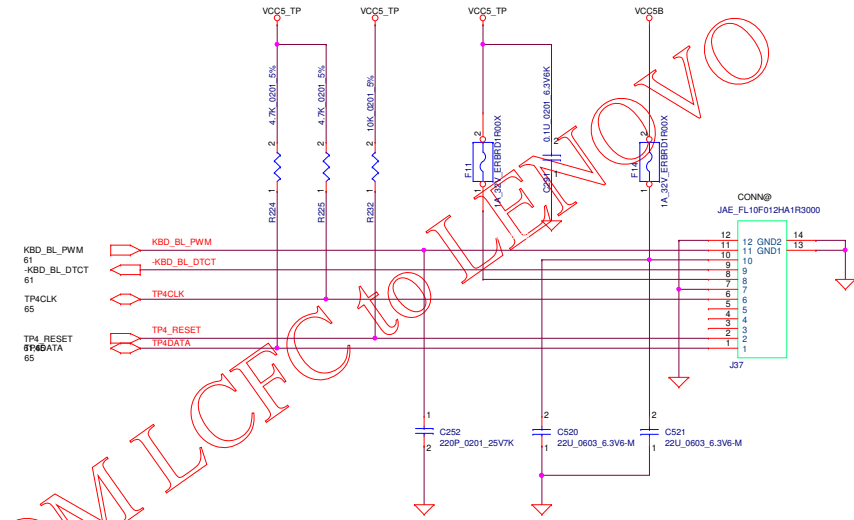
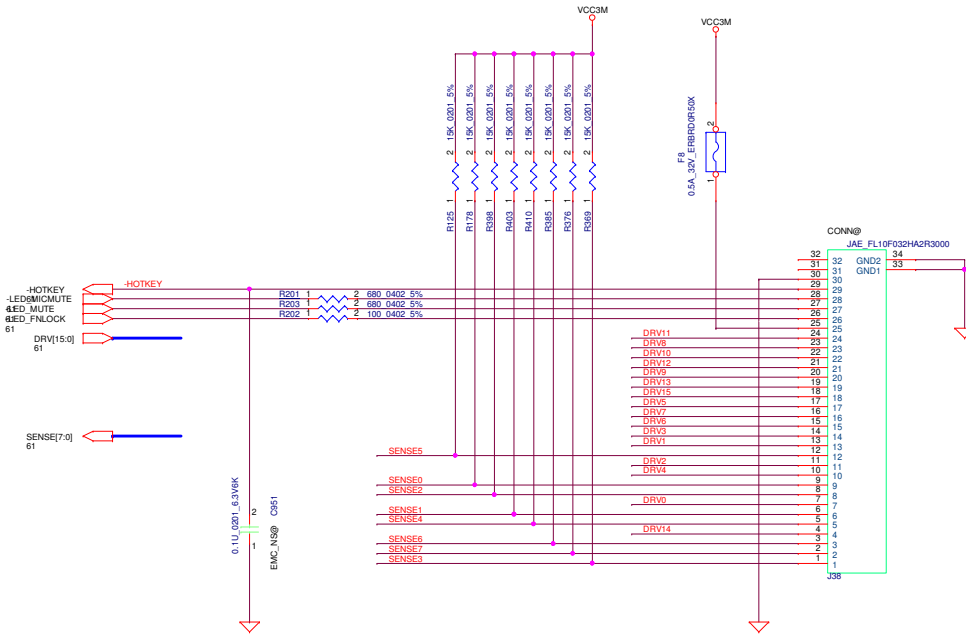


TABLE

Sensor	Device	Placed on
DIODE 0	EC Internal	BOTTOM
DIODE 1	CPU DC-DC	BOTTOM
DIODE 2	DIAM	BOTTOM
DIODE 3	WLAM	BOTTOM
DIODE 4	#GFX DC-DC	BOTTOM
DIODE 5	Onboard DRAM	BOTTOM
DIODE 6	WWAN	BOTTOM

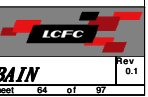


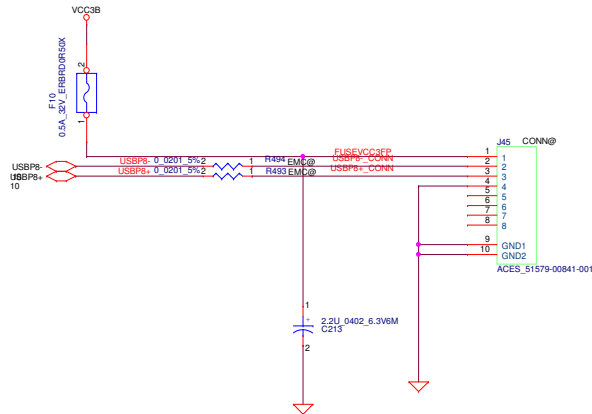
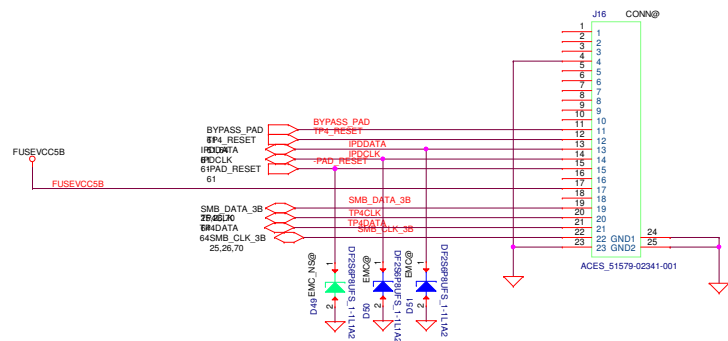
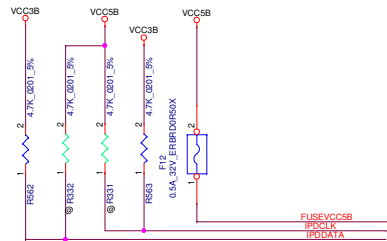
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2014/08/10		2015/08/10		Doc Number	
2014/08/10		2015/08/10		CORALINS	
2014/08/10		2015/08/10		Rev	
2014/08/10		2015/08/10		6.1	



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				Date	Thursday, October 16, 2015
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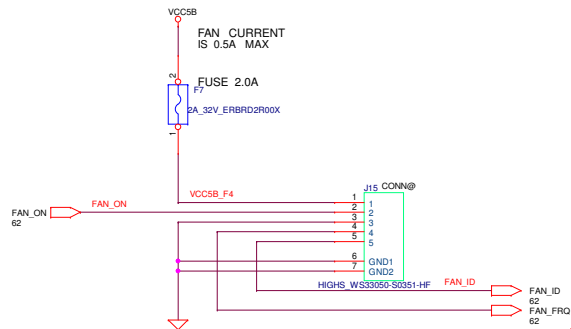
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				Custom	COBAIN SWG	0.1	
				Date:	Thursday, October 15, 2015	Sheet	66 of 97

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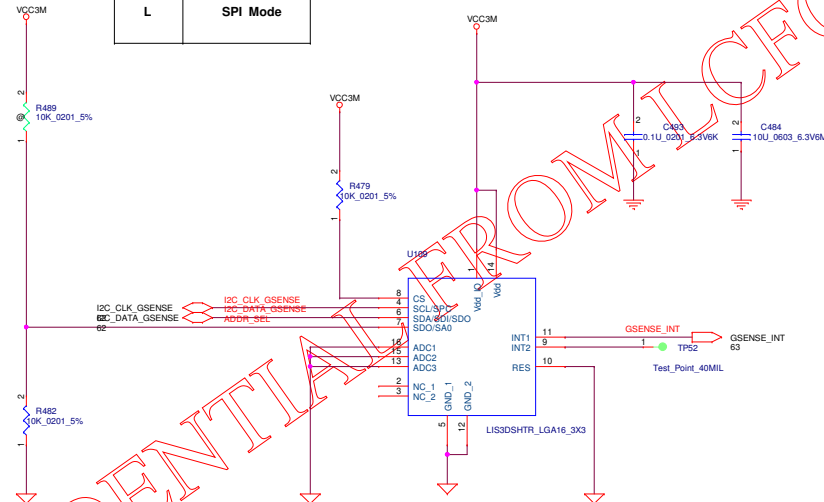
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				Rev 0.1
				Date: Thursday, October 15, 2015 Sheet 67 of 97

TABLE

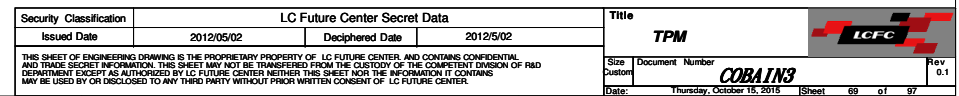
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KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

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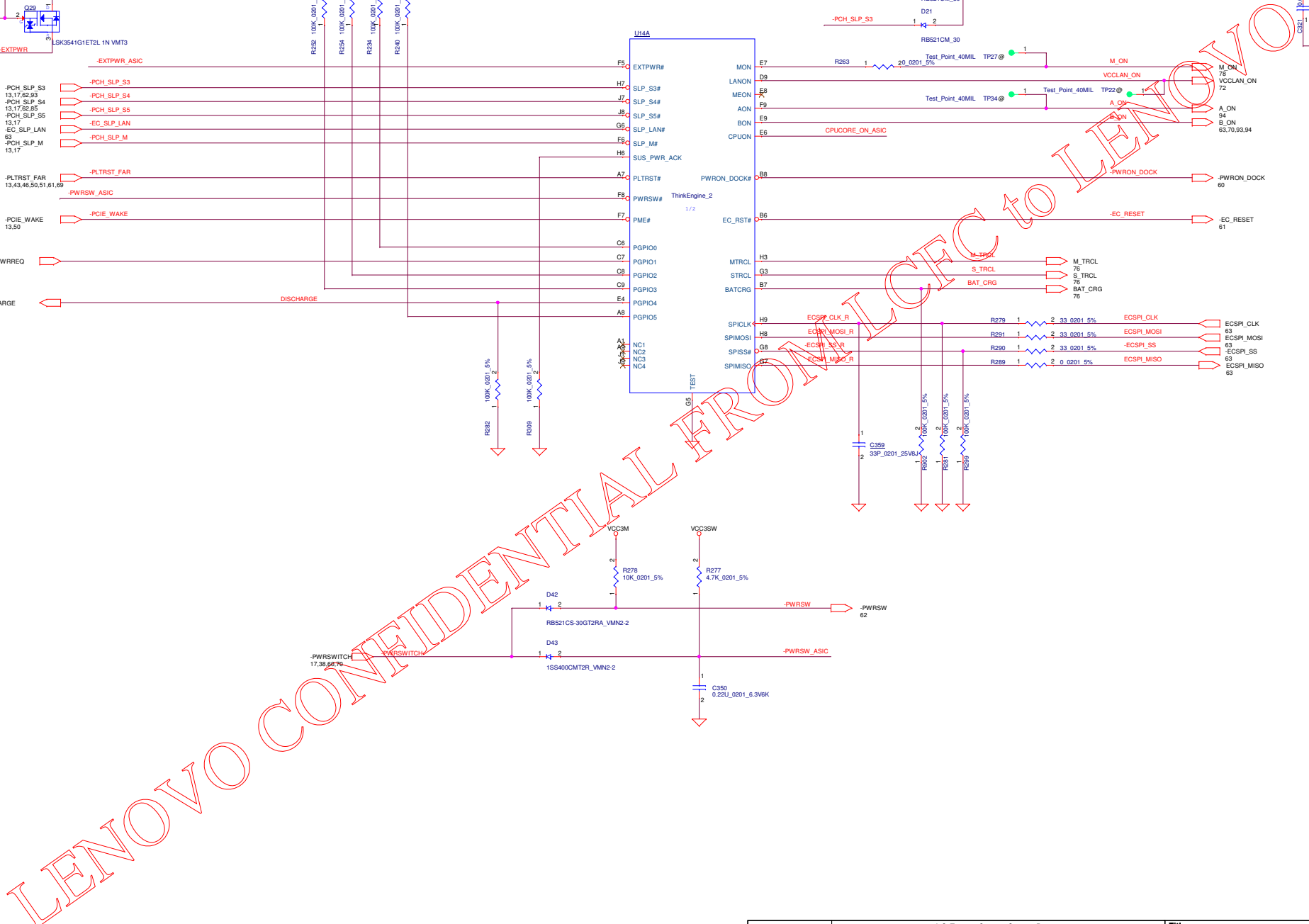
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H	I2C Mode
L	SPI Mode



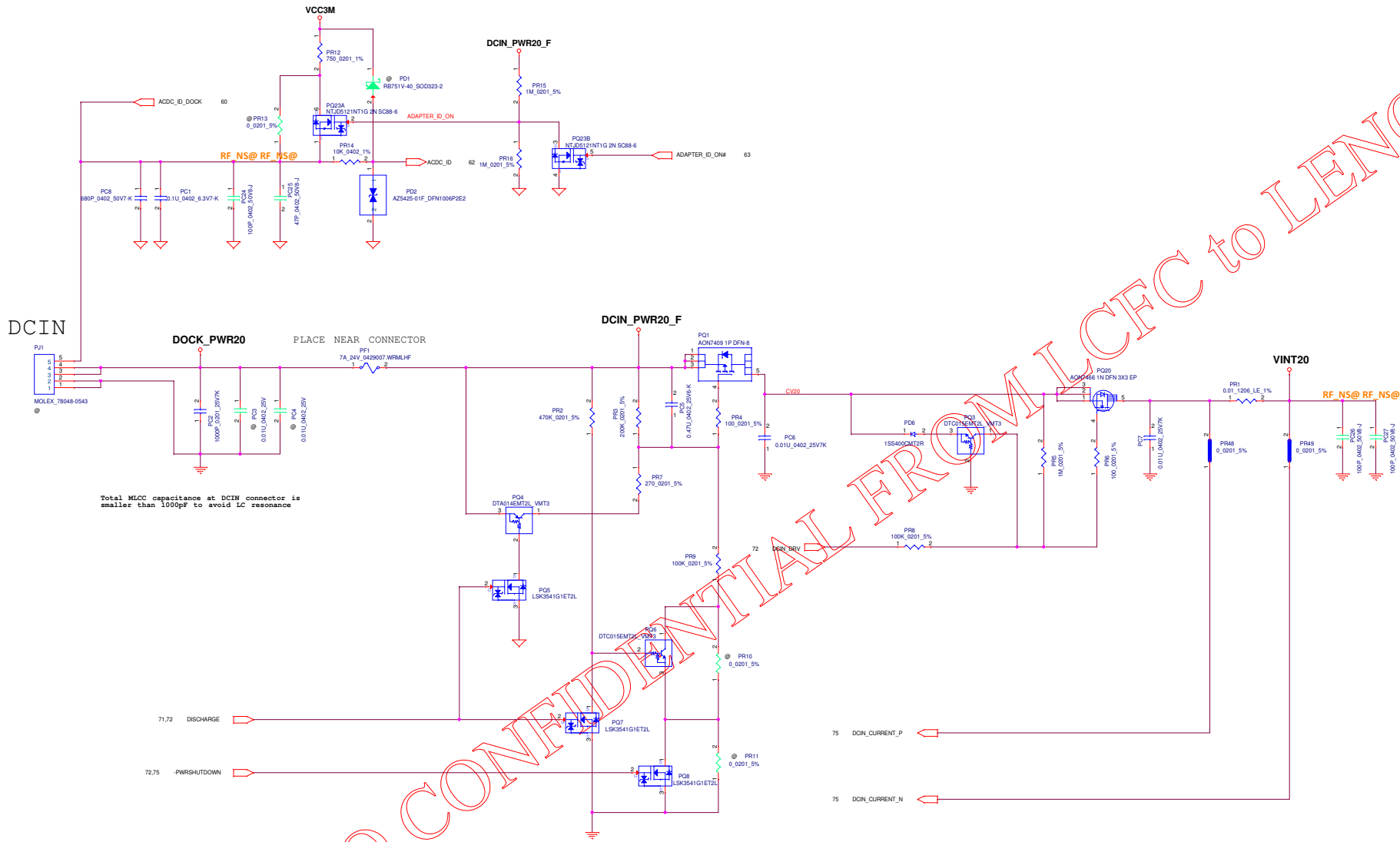












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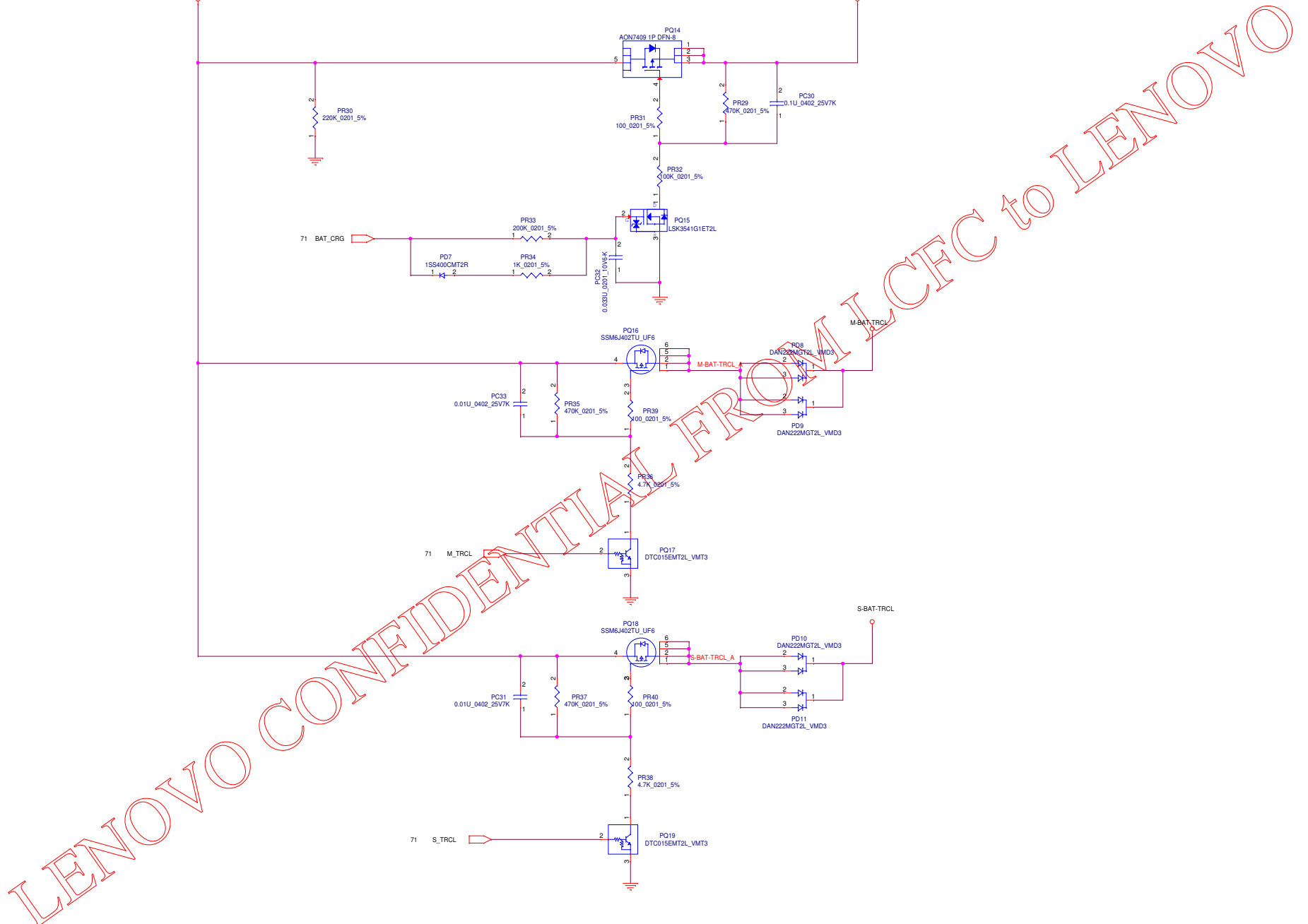
PEAK SHIFT	YES	NO
RR10	NO-ASM	ASM
PR2	ASM	NO-ASM
PQ7	ASM	NO-ASM
PQ6	ASM	NO-ASM

↑  
LOGIC

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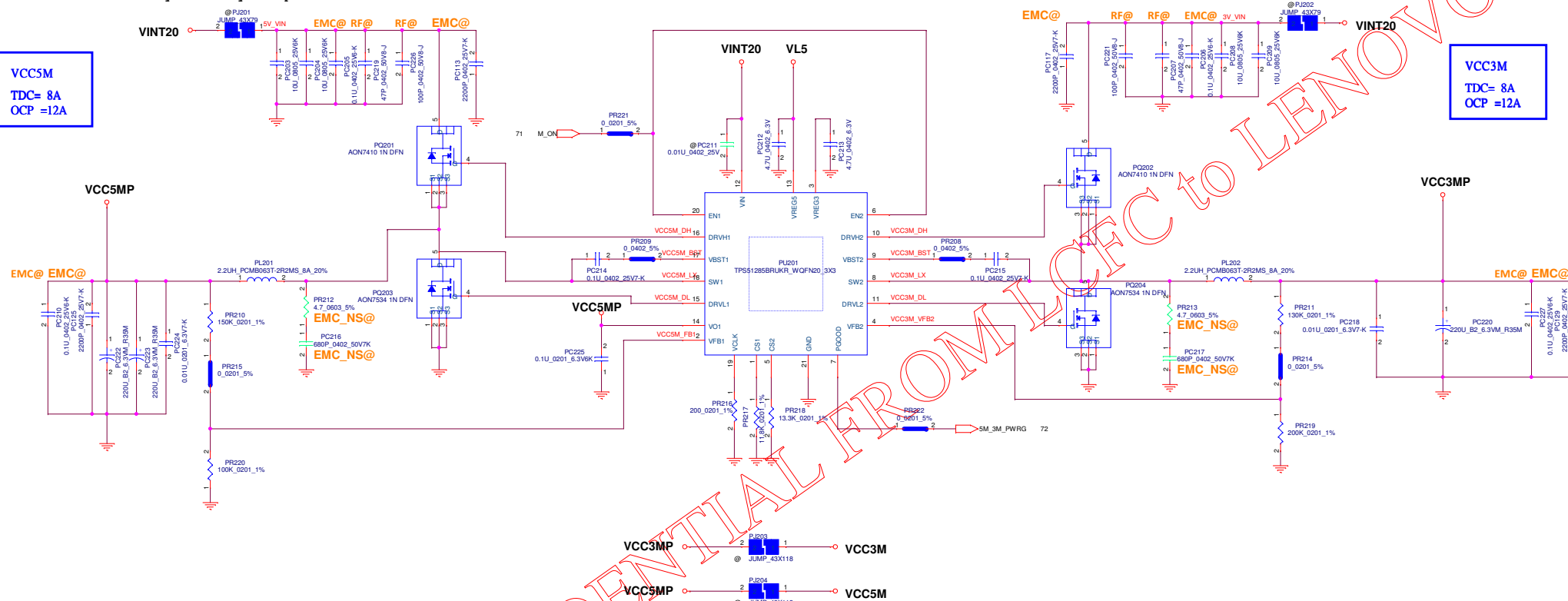
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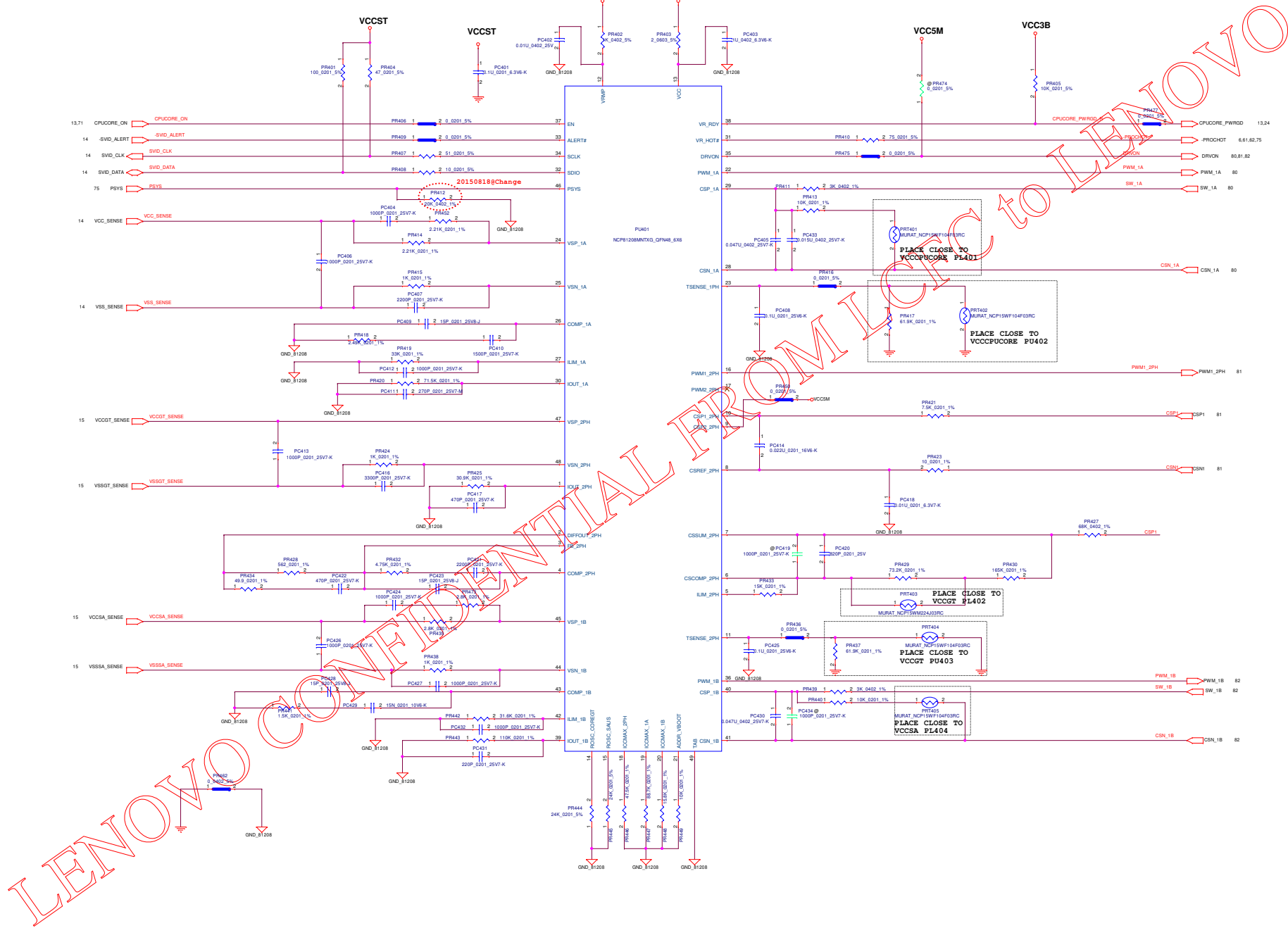
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				<small>Date:</small> Thursday, October 15, 2015		<small>Sheet</small> 77 of 95	

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0.24

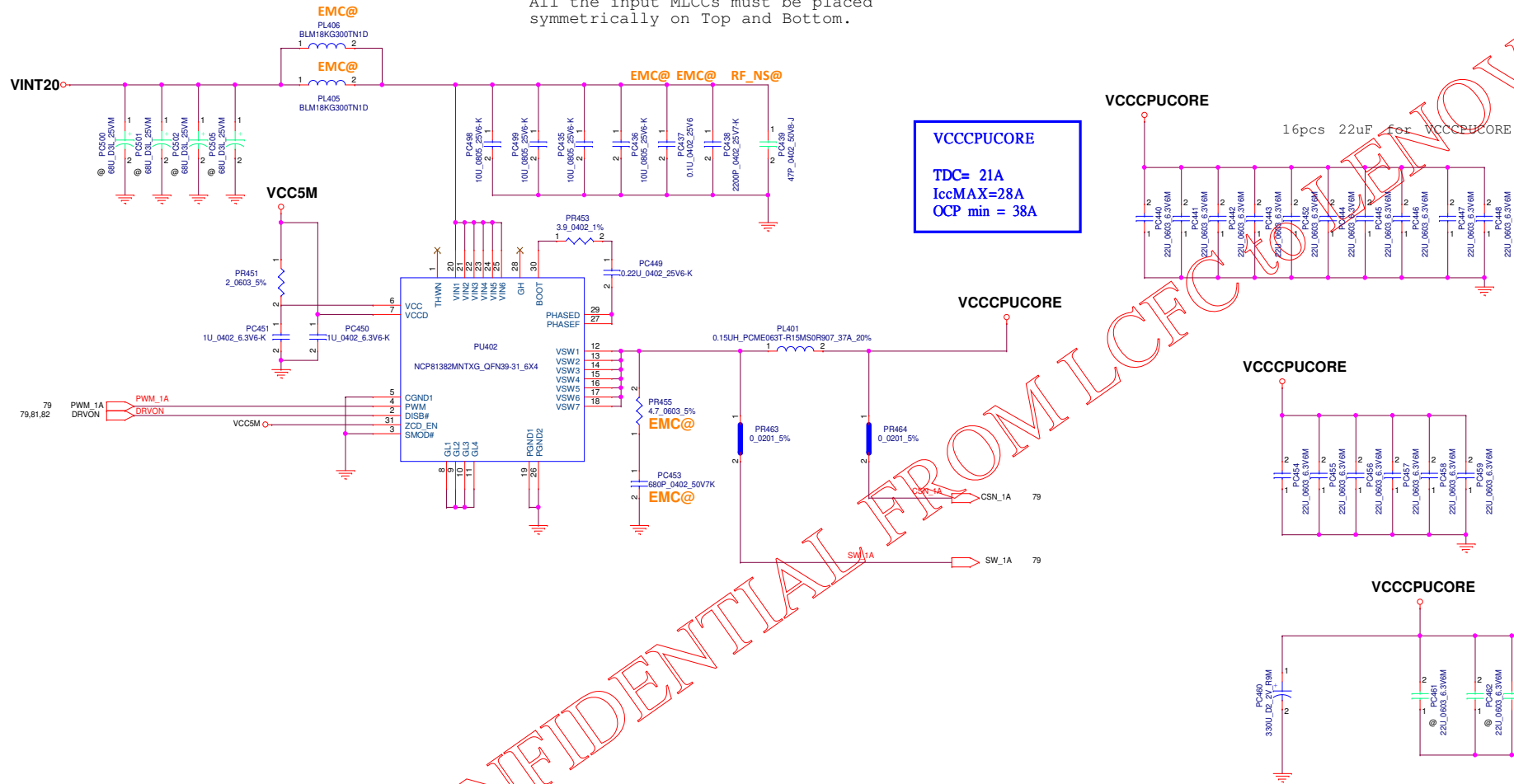
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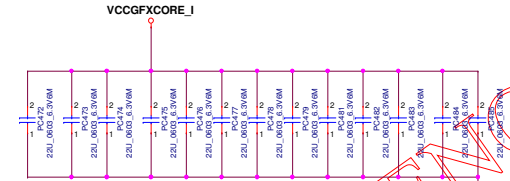
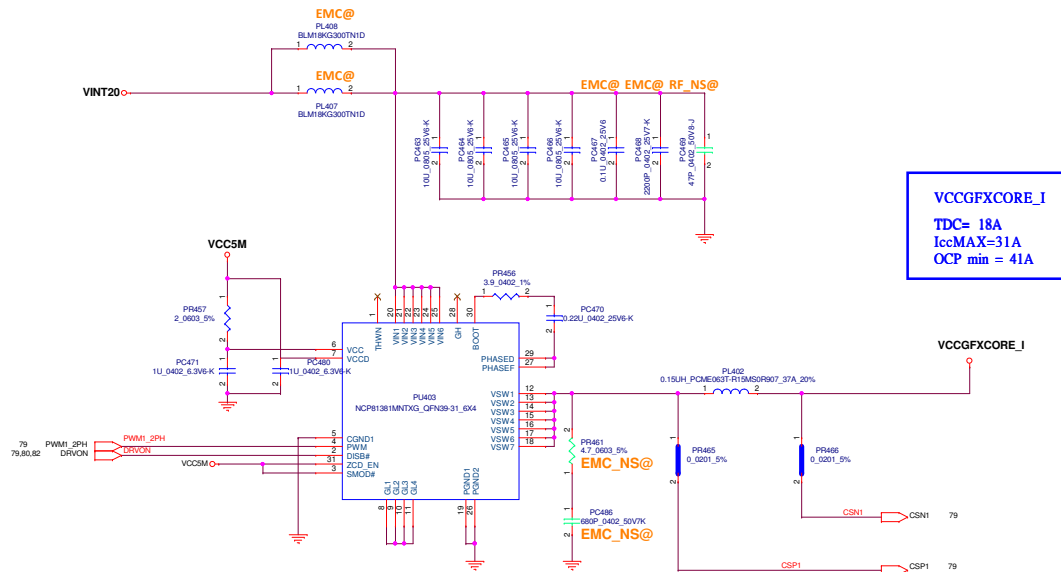
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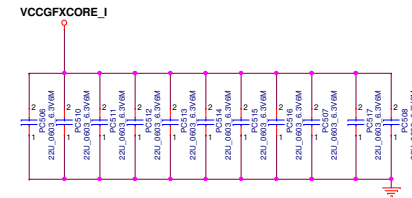
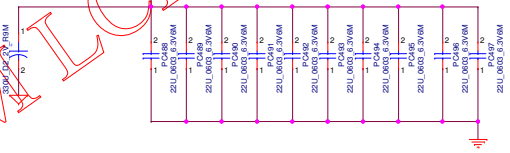
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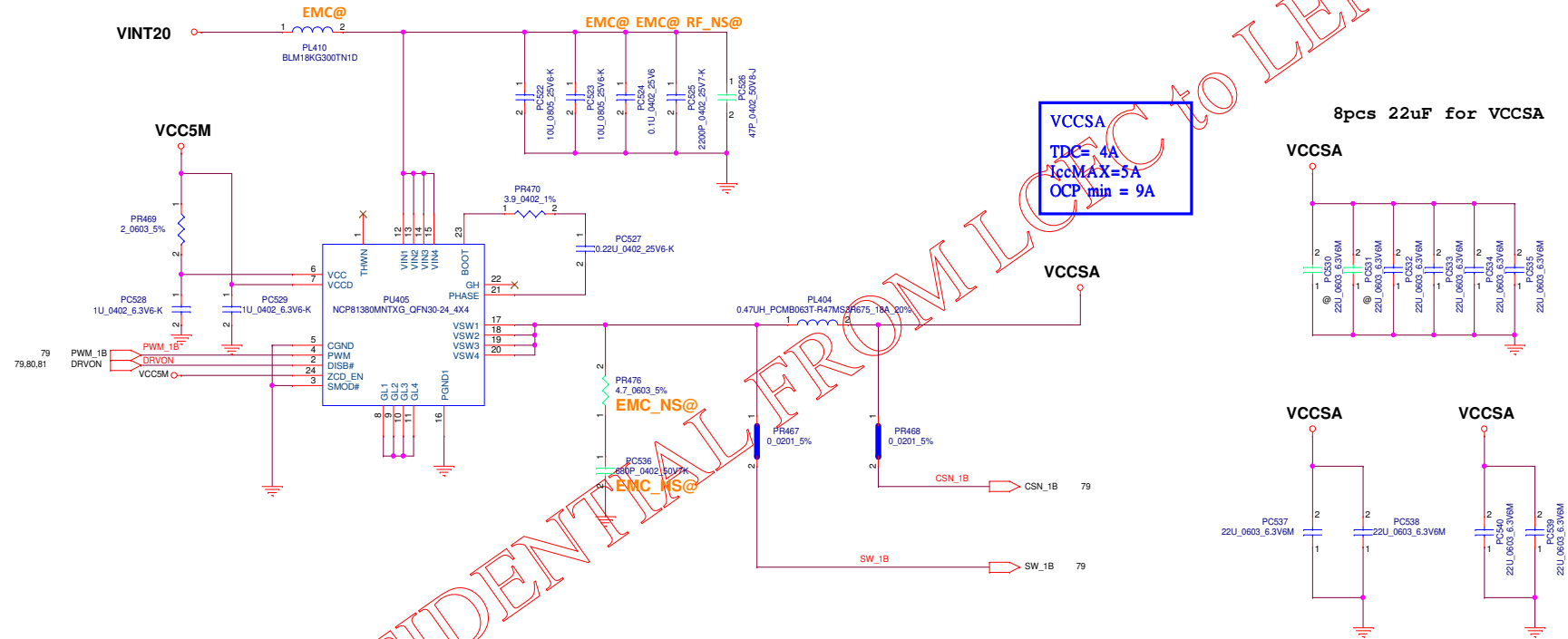



VCCGFXCORE\_I 34pcs 22uF for VCCGFXCORE\_I

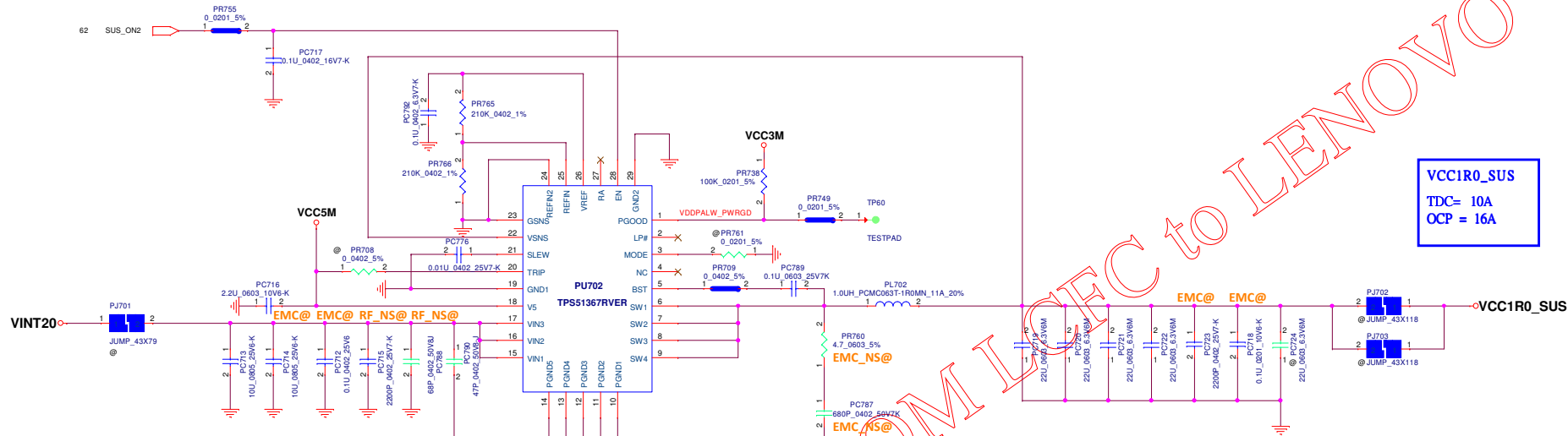


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				0.1	
Size	Document	Number		Cobain3 Intel	
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VCC1R0\_SUS  
TDC= 10A  
OCP = 16A

Mode	Frequency
GND	400KHz
Float	800KHz

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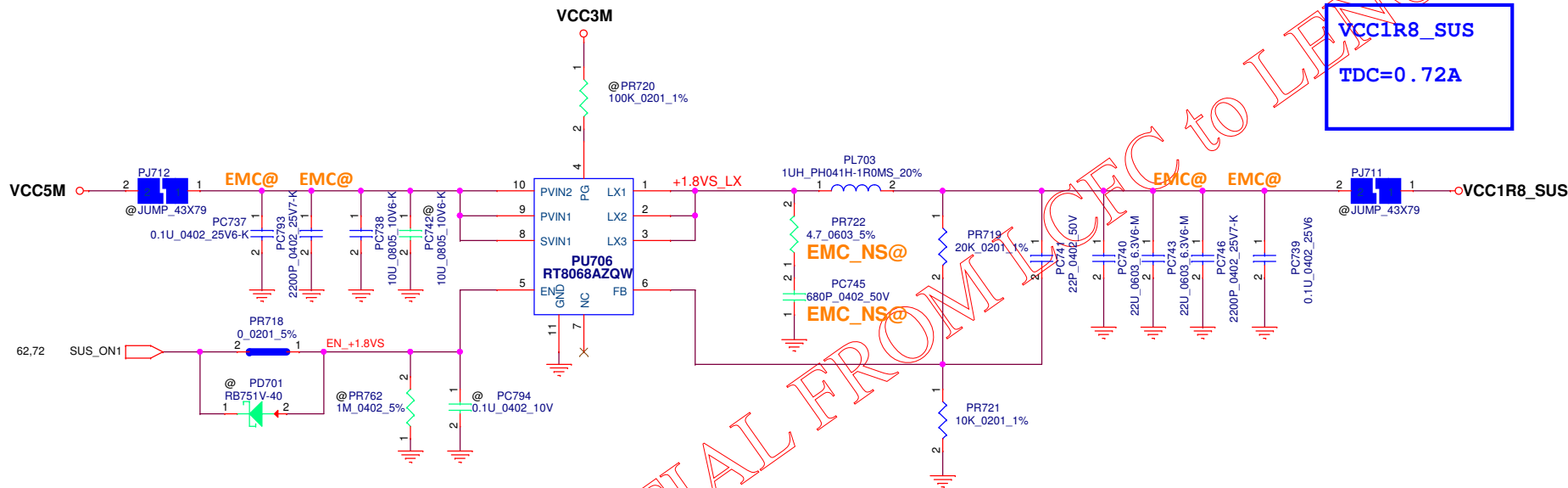
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			Date:	Thursday, October 15, 2015	Sheet 84 of 95




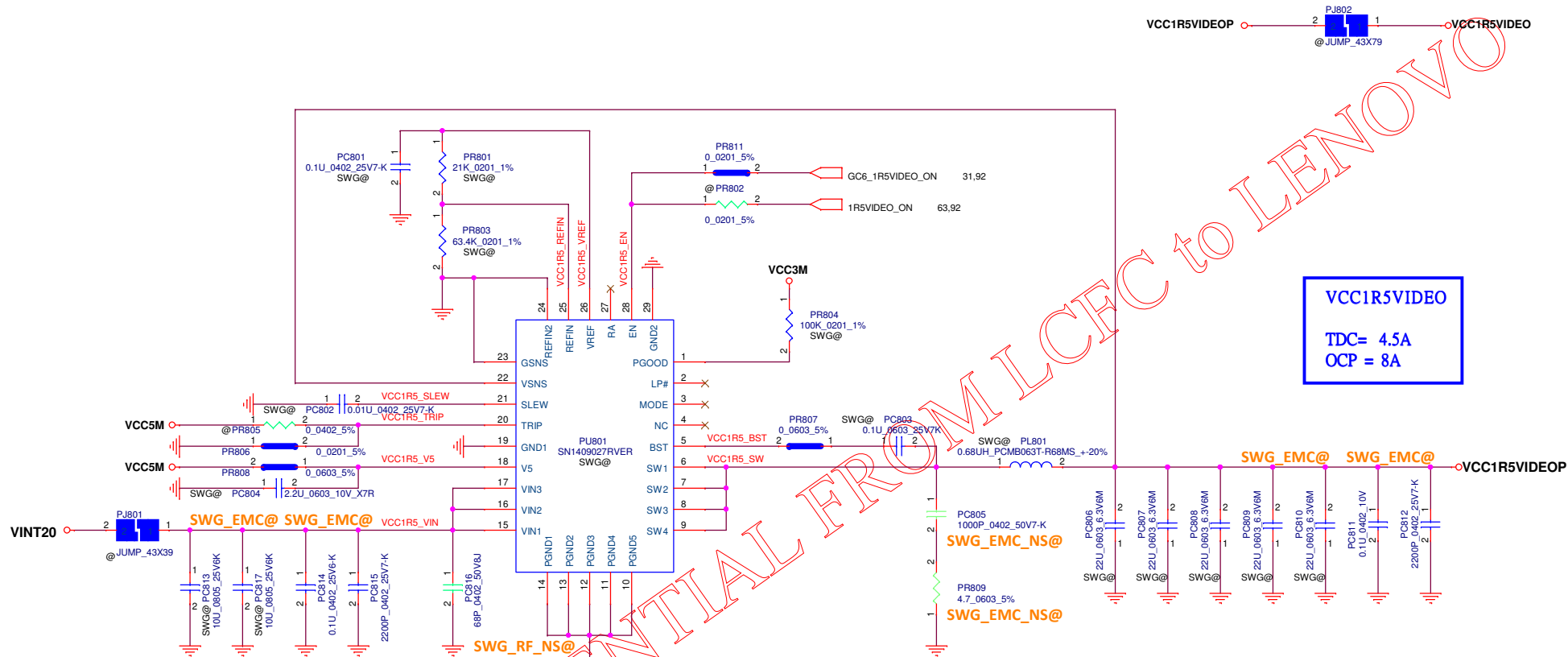




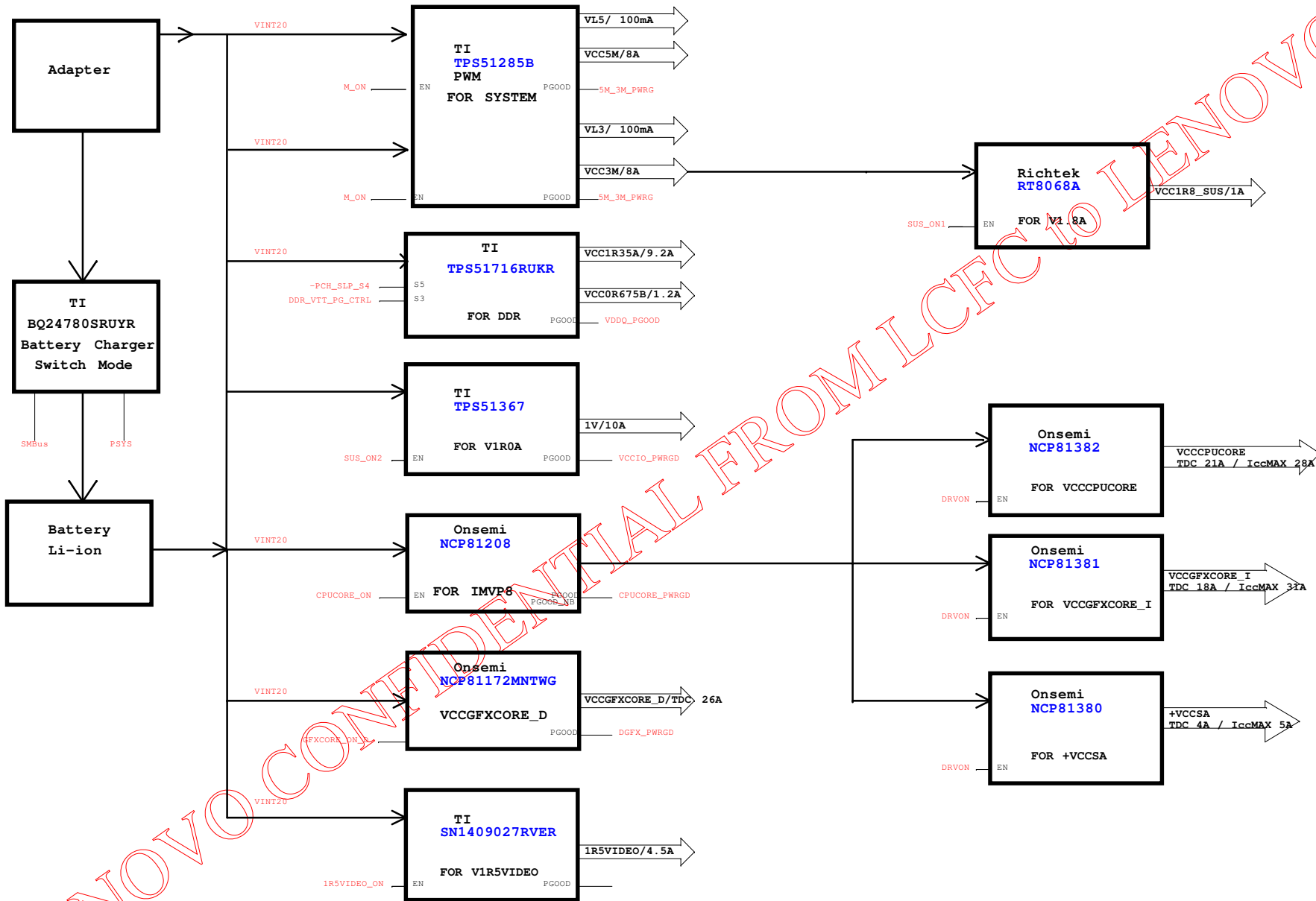
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VCCGFXCORE\_D  
TDC= 26A  
EDR-PEAK=51A  
OCP = 58A

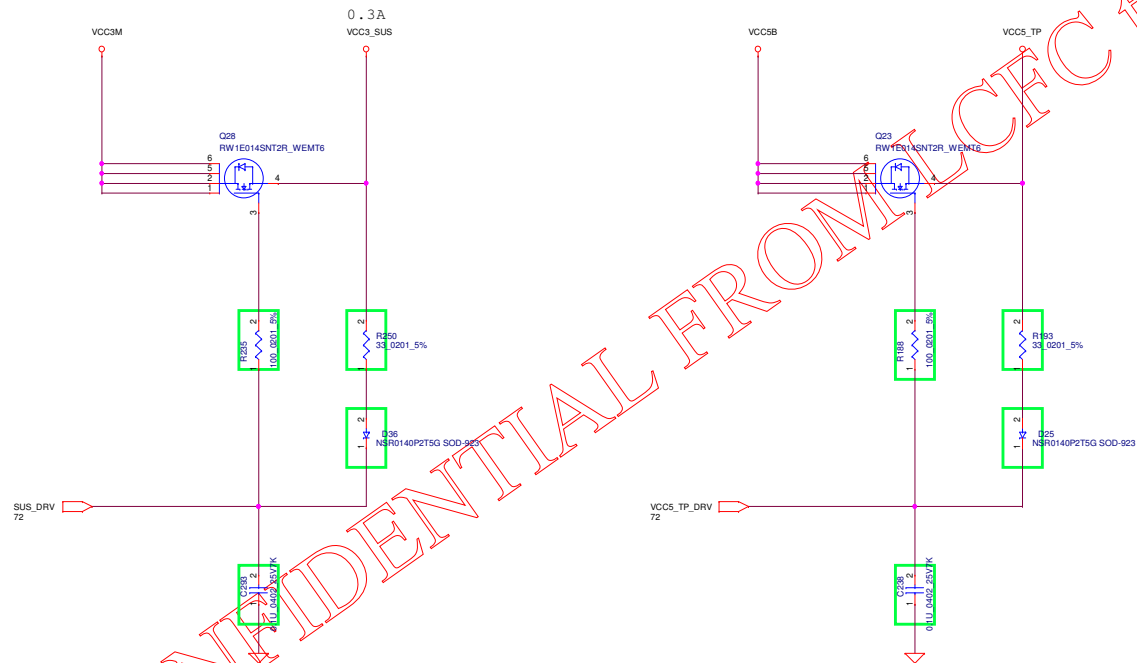
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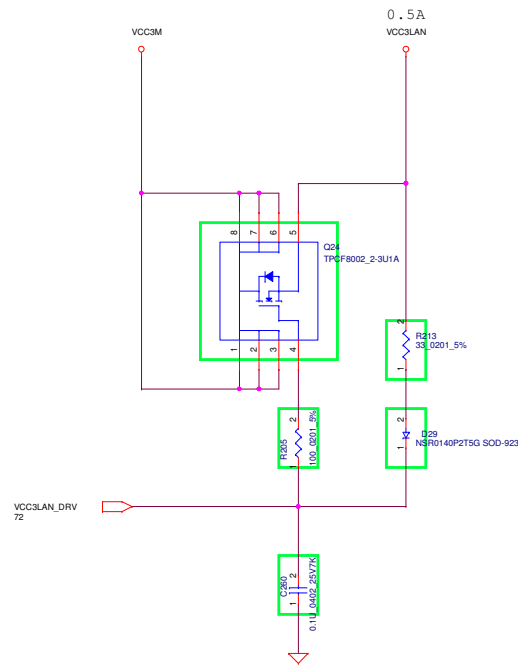
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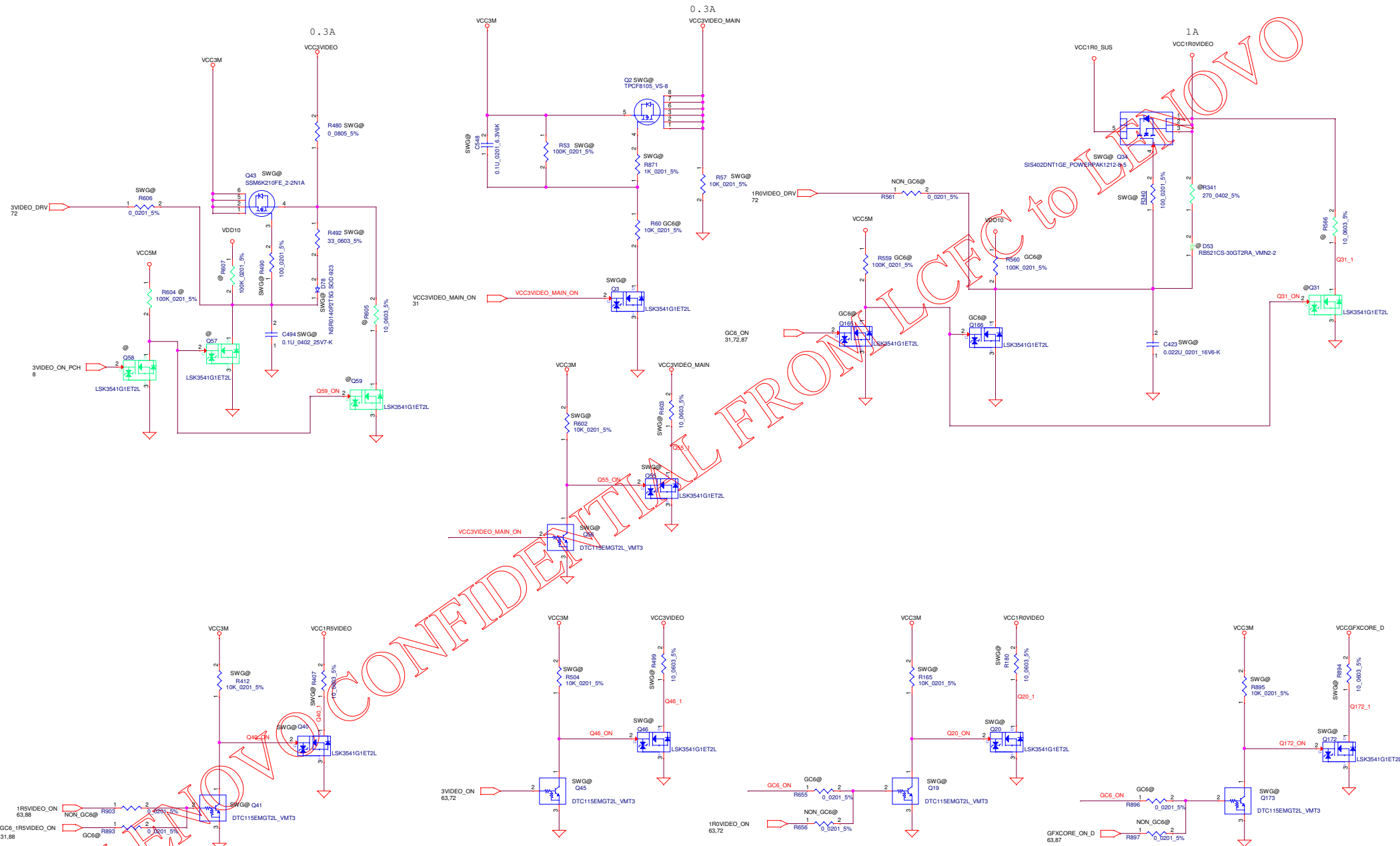



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2012/11/01		2013/12/31		Cobain SWG	
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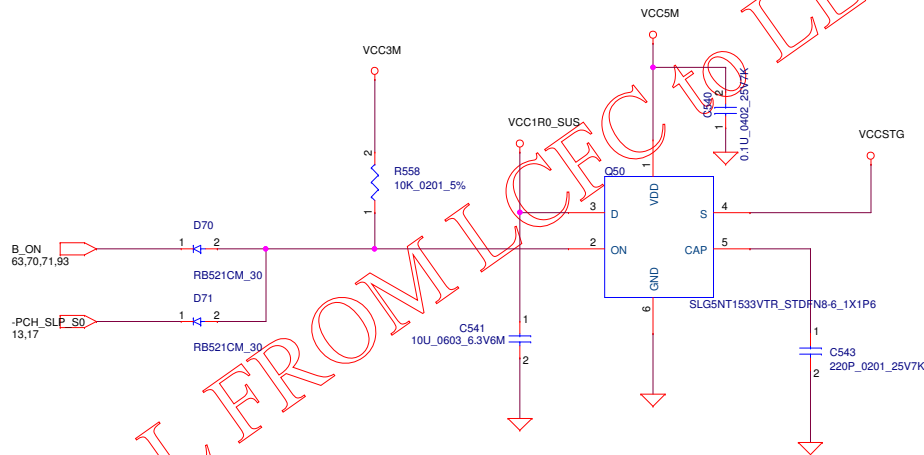
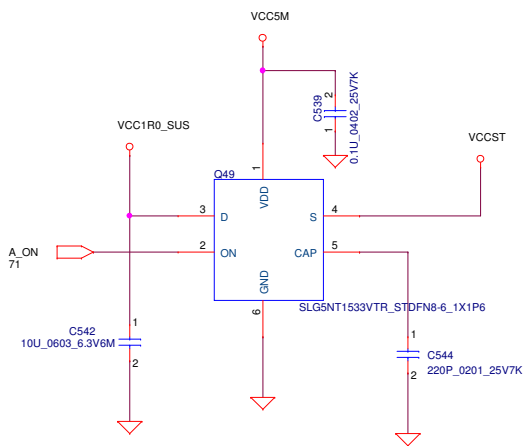
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				Date	COBAIN3	0.24
				Date	Friday, October 16, 2015	Sheet
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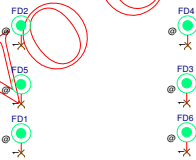
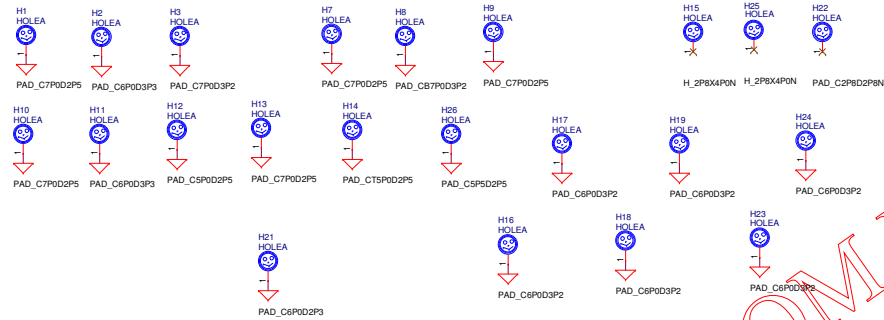
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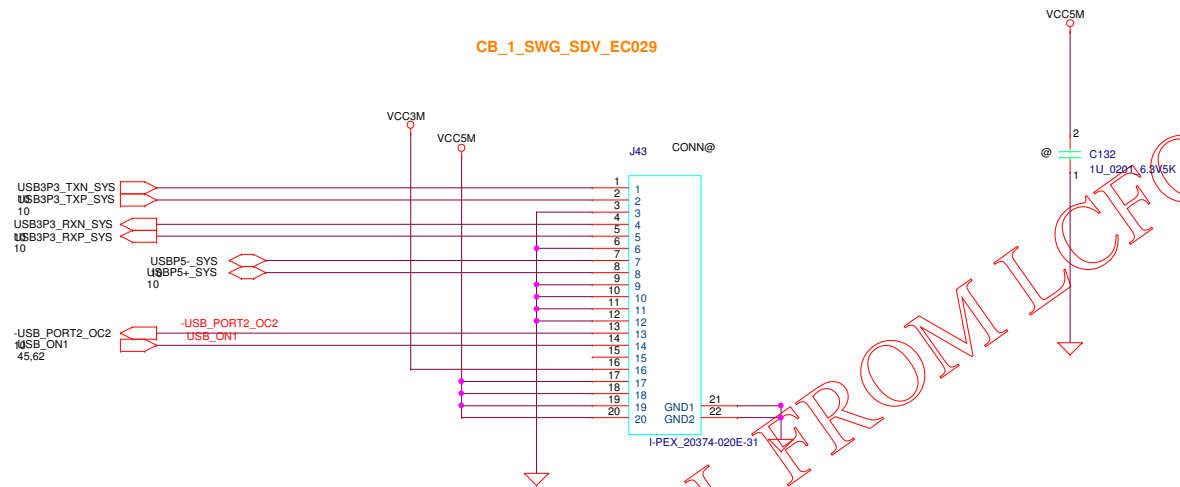
FID  
Board Area


FID  
Component Area



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